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ILI2303

ILI2303
Capacitive Touch Sensor Controller

Specification

Version: V1.03

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ILI TECHNOLOGY CORP.
8F, No.38, Taiyuan St., Jhubei City, Hsinchu County 302, Taiwan, R.O.C.
Tel.886-3-5600099; Fax.886-3-5600055
http://www.ilitek.com

Revision History

Version No.	Date	Page	Description
V0.00	2012/8/27		Draft specification
V0.01	2013/1/22		Preliminary specification
V0.02	2013/2/8		Modify pin description
V0.03	2013/3/21		1. Modify pin 87 and 88 description. 2. Modify typical application circuit.
V0.04	2013/9/5		1. Modify pin description. 2. Modify typical application circuit.
V1.00	2014/7/28		Formal specification
V1.01	2014/9/5		Add power consumption.
V1.02	2014/9/5		Add I2C timing characteristics.
V1.03	2014/9/17		Add typical voltage condition and digital I/O electrical characteristic

CONTENT

1. Description

The ILI2303 is a single chip capacitive touch sensor controller optimized for Tablet and NB touch panel design. It integrates with specialized 32-bit MCU, high speed CDC (capacitance to digital converter), 68-ch high voltage driving and sensing I/O channels and high voltage charge pump controller in a compact 88-pin QFN 10mm*10mm*0.8mm package. It supports I2C host control interface. It also meets Windows 8 requirements with best human touch performance.

2. Features

- 68 channels for capacitive touch panel.
- Flexible driving or sensing channel assignment
- Programmable driving voltage with skew control for driving channels
- High speed ADC with programmable 8-bit or 10-bit resolution
- Support auto baseline calibration circuit
- Support smart edge sensing
- Support smart touch detection
- Built-in noise processing function
- High speed 32-bit micro-controller
- Up to 1MHz I2C slave device
- High voltage charge pump controller with programmable clamp voltage function
- Input voltage low level detection circuit
- Input voltage power on reset circuit
- Support power down mode
- Driving to Sensing mutual capacitance: 1pF to 4pF

3. Block Diagram

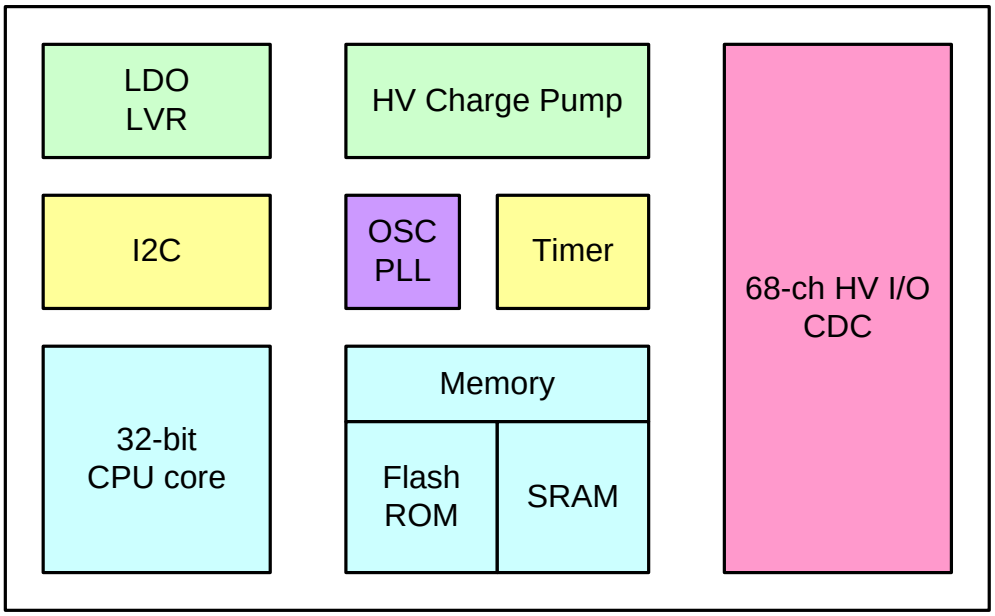
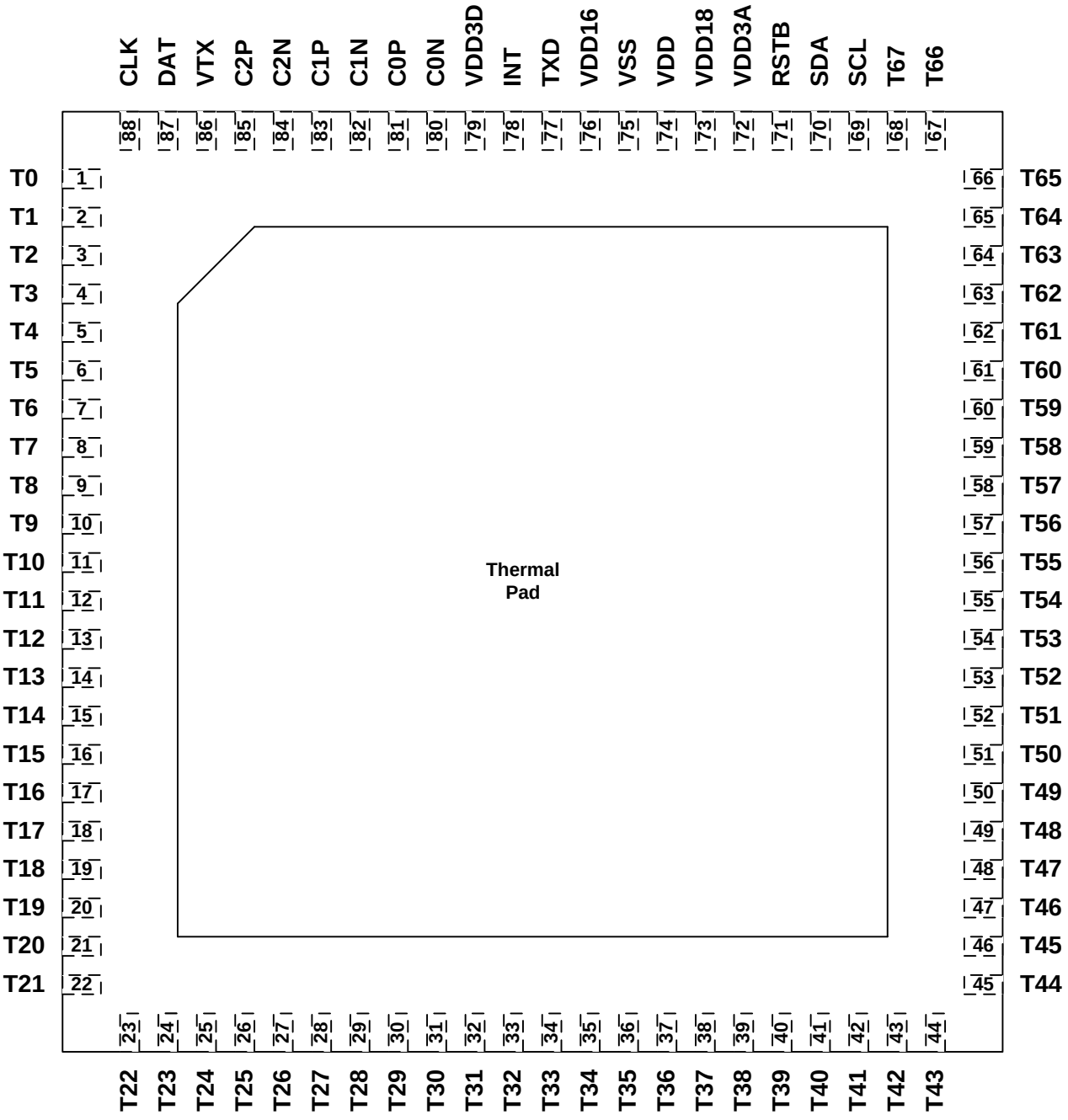


Figure 3-1: ILI2303 Block Diagram

4. Pin Definition

4.1 QFN-88 Pin Assignment

Top View



4.2 Pin Description

QFN-88 Pin Description

Pin No.	Pin Name	Pin Type*	Description
1	T0	I/O	HV I/O channel 0
2	T1	I/O	HV I/O channel 1
3	T2	I/O	HV I/O channel 2
4	T3	I/O	HV I/O channel 3
5	T4	I/O	HV I/O channel 4
6	T5	I/O	HV I/O channel 5
7	T6	I/O	HV I/O channel 6
8	T7	I/O	HV I/O channel 7
9	T8	I/O	HV I/O channel 8
10	T9	I/O	HV I/O channel 9
11	T10	I/O	HV I/O channel 10
12	T11	I/O	HV I/O channel 11
13	T12	I/O	HV I/O channel 12
14	T13	I/O	HV I/O channel 13
15	T14	I/O	HV I/O channel 14
16	T15	I/O	HV I/O channel 15
17	T16	I/O	HV I/O channel 16
18	T17	I/O	HV I/O channel 17
19	T18	I/O	HV I/O channel 18
20	T19	I/O	HV I/O channel 19
21	T20	I/O	HV I/O channel 20
22	T21	I/O	HV I/O channel 21
23	T22	I/O	HV I/O channel 22
24	T23	I/O	HV I/O channel 23
25	T24	I/O	HV I/O channel 24
26	T25	I/O	HV I/O channel 25
27	T26	I/O	HV I/O channel 26
28	T27	I/O	HV I/O channel 27
29	T28	I/O	HV I/O channel 28
30	T29	I/O	HV I/O channel 29
31	T30	I/O	HV I/O channel 30
32	T31	I/O	HV I/O channel 31
33	T32	I/O	HV I/O channel 32
34	T33	I/O	HV I/O channel 33
35	T34	I/O	HV I/O channel 34

Pin No.	Pin Name	Pin Type*	Description
36	T35	I/O	HV I/O channel 35
37	T36	I/O	HV I/O channel 36
38	T37	I/O	HV I/O channel 37
39	T38	I/O	HV I/O channel 38
40	T39	I/O	HV I/O channel 39
41	T40	I/O	HV I/O channel 40
42	T41	I/O	HV I/O channel 41
43	T42	I/O	HV I/O channel 42
44	T43	I/O	HV I/O channel 43
45	T44	I/O	HV I/O channel 44
46	T45	I/O	HV I/O channel 45
47	T46	I/O	HV I/O channel 46
48	T47	I/O	HV I/O channel 47
49	T48	I/O	HV I/O channel 48
50	T49	I/O	HV I/O channel 49
51	T50	I/O	HV I/O channel 50
52	T51	I/O	HV I/O channel 51
53	T52	I/O	HV I/O channel 52
54	T53	I/O	HV I/O channel 53
55	T54	I/O	HV I/O channel 54
56	T55	I/O	HV I/O channel 55
57	T56	I/O	HV I/O channel 56
58	T57	I/O	HV I/O channel 57
59	T58	I/O	HV I/O channel 58
60	T59	I/O	HV I/O channel 59
61	T60	I/O	HV I/O channel 60
62	T61	I/O	HV I/O channel 61
63	T62	I/O	HV I/O channel 62
64	T63	I/O	HV I/O channel 63
65	T64	I/O	HV I/O channel 64
66	T65	I/O	HV I/O channel 65
67	T66	I/O	HV I/O channel 66
68	T67	I/O	HV I/O channel 67
69	SCL	I	Input clock signal of I2C. Connect a resistor 4.7kΩ to VDD3D.
70	SDA	I/O	Output data signal of I2C. Connect a resistor 4.7kΩ to VDD3D.
71	RSTB	I	Input reset signal of MCU. Low active reset.
72	VDD3A	P	Input power supply. Connect a bypass capacitor 2.2uF to GND.

Pin No.	Pin Name	Pin Type*	Description
73	VDD18	P	Output power supply of internal LDO. Connect a bypass capacitor 4.7uF to GND.
74	VDD	P	Input power supply. Connect a bypass capacitor 4.7uF to GND.
75	VSS	P	Digital circuit reference ground. Connect to GND.
76	VDD16	P	Output power supply of internal LDO. Connect a bypass capacitor 2.2uF to GND.
77	TXD	O	Output data signal for test.
78	INT	O	Output interrupt signal for host controller.
79	VDD3D	P	Input power supply. Connect a bypass capacitor 2.2uF to GND.
80	C0N	O	Output clock signal of charge pump. Connect a fly capacitor 0.1uF/50V/X7R to C0P.
81	C0P	O	Output clock signal of charge pump. Connect a fly capacitor 0.1uF/50V/X7R to C0N.
82	C1N	O	Output clock signal of charge pump. Connect a fly capacitor 0.1uF/50V/X7R to C1P.
83	C1P	O	Output clock signal of charge pump. Connect a fly capacitor 0.1uF/50V/X7R to C1N.
84	C2N	O	Output clock signal of charge pump. Connect a fly capacitor 0.1uF/50V/X7R to C2P.
85	C2P	O	Output clock signal of charge pump. Connect a fly capacitor 0.1uF/50V/X7R to C2N.
86	VTX	O	Output power supply of charge pump. Connect a bypass capacitor 0.1uF/50V/X7R to GND.
87	DAT	I/O	Input data signal of ICE.
88	CLK	I	Input clock signal of ICE.
Thermal Pad	AGND	P	Analog circuit reference ground. Connect to GND.

*Pin type: P=power or ground; I=input only; O=output only (push-pull); I/O=bi-direction

5. Electrical Characteristics

5.1 Absolute Maximum Ratings (Note 1,2)

Parameter	Symbol	Min	Max	Unit
VDD to GND	VDD	-0.3	6.5	V
VDD18 to GND	VDD18	-0.3	3.6	V
VDD3D	VDD3D	-0.3	3.6	V
VDD3A	VDD3A	-0.3	3.6	V
VDD16 to GND	VDD16	-0.3	1.65	V
VTX to GND	VTX	-0.3	35	V
ESD Susceptibility HBM (Human Body Mode) **(Note 2)**	HBM		2000	V
ESD Susceptibility MM (Machine Mode)	MM		200	V

Note 1: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2: Devices are ESD sensitive. Handling precaution is recommended.

5.2 Recommended Operating Conditions (Note 3)

Parameter	Symbol	Min	Typ.	Max	Unit
VDD to GND	VDD	2.7	3.0	5.5	V
VDD3D	VDD3D	2.7	3.0	3.3	V
VDD3A	VDD3A	2.7	3.0	3.3	V
Operating Ambient Temperature Range	T_A	-40	27	85	℃
Operating Junction Temperature Range	T_J	-40	27	125	℃
Storage Ambient Temperature Range	T_{ST}	-40	27	150	℃

Note 3: The device is not guaranteed to function outside its operating conditions.

5.3 Digital IO DC Electrical Characteristic

Parameter	Symbol	Min	Typ.	Max	Unit
VOH output High (driven)	VOH	0.7VDD3D			V
VOL output Low (driven)	VOL			0.3VDD3D	V
VIH input high	VIH	0.65VDD3D		VDD3D+0.5	V
VIL input low	VIL	-0.5		0.3VDD3D	V

5.3 Power Consumption (Note 4)

Parameter	Symbol	Typ.	Unit
Input Power Supply	VDD	3.3	V
Active Current	I_{ACT}	60	mA
Idle Current	I_{IDL}	40	mA

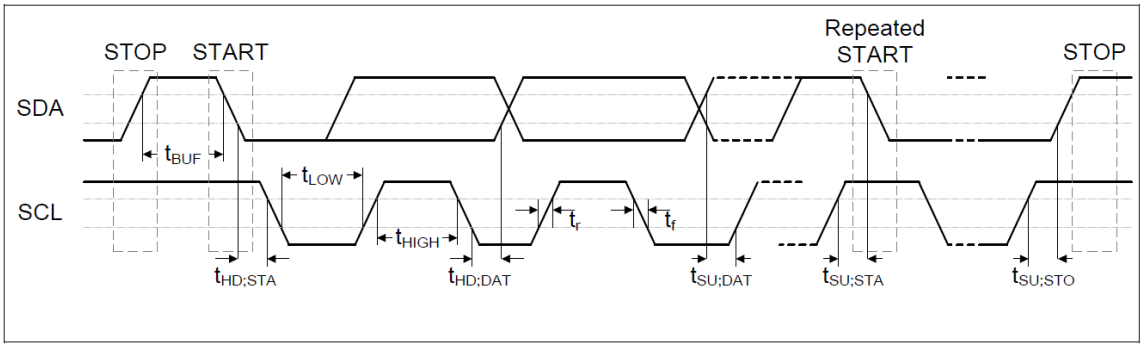
Note 4: The active current was measured under 100Hz report rate with 10 fingers touching. The touch panel size is 15.6 inch GFF type sensor.

5.4 I2C Interface Operating Conditions

5.4.1 I2C DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Max	Unit
Input high (driven)	V_{IH}		-0.5	$0.3V_{DD}$	V
Input low	V_{IL}		$0.7V_{DD}$		V
hysteresis of Schmitt trigger inputs	V_{hys}		$0.05V_{DD}$		V
LOW-level output voltage 1	V_{OL1}	(open-drain or open-collector) at 3 mA sink current; V_{DD} > 2 V	0	0.4	V
LOW-level output voltage 2	V_{OL2}	(open-drain or open-collector) at 2 mA sink current[3]; V_{DD} <= 2 V	0	$0.2V_{DD}$	V
LOW-level output current	I_{OL}	V_{OL} = 0.4 V	20		mA
output fall time from V_{IHmin} to V_{ILmax}	t_{of}		20 x (V_{DD} / 5.5 V)[	120	ns
pulse width of spikes that must be suppressed by the input filter	t_{SP}		0	50	ns
input current each I/O pin	I_i	$0.1V_{DD} < V_I < 0.9V_{DDmax}$	-10	+10	uA
capacitance for each I/O pin	C_i			10	pF

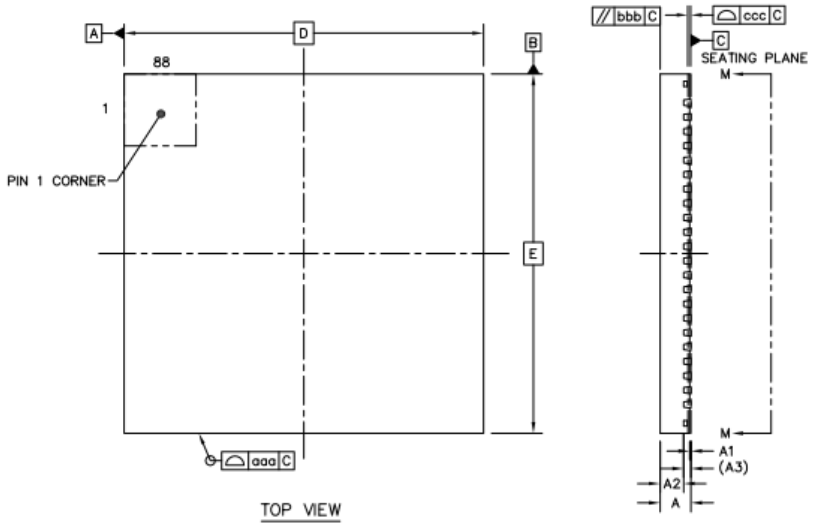
5.4.2 I2C Bus Timing

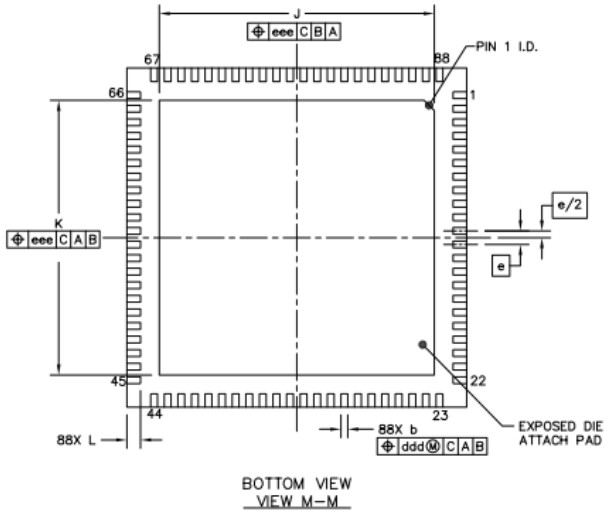


Parameter	Symbol	Conditions	Min	Max	Unit
SCL clock frequency	f_{SCL}			1000	kHz
hold time (repeated) START condition	$t_{HD;STA}$	After this period, the first clock pulse is generated.	0.26		us
LOW period of the SCL clock	t_{LOW}		0.5		us
HIGH period of the SCL clock	t_{HIGH}		0.26		us
set-up time for a repeated START condition	$t_{SU;STA}$		0.26		us
data hold time	$t_{HD;DAT}$	I2C-bus devices	0		us
rise time of both SDA and SCL signals	t_r			120	ns
fall time of both SDA and SCL signals	t_f		20x(V_{DD} / 5.5 V)	120	ns
set-up time for STOP condition	$t_{SU;STO}$		0.26		us
bus free time between a STOP and START condition	t_{BUF}		0.5		us
capacitive load for each bus line	C_b		0.5		us
data valid time	$t_{VD;DAT}$			0.45	us

6. Package Information

6.1 QFN-88 Package Dimension





		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		10 BSC	
	Y	E		10 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	8	8.1	8.2
	Y	K	8	8.1	8.2
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

7. Typical Application Circuit

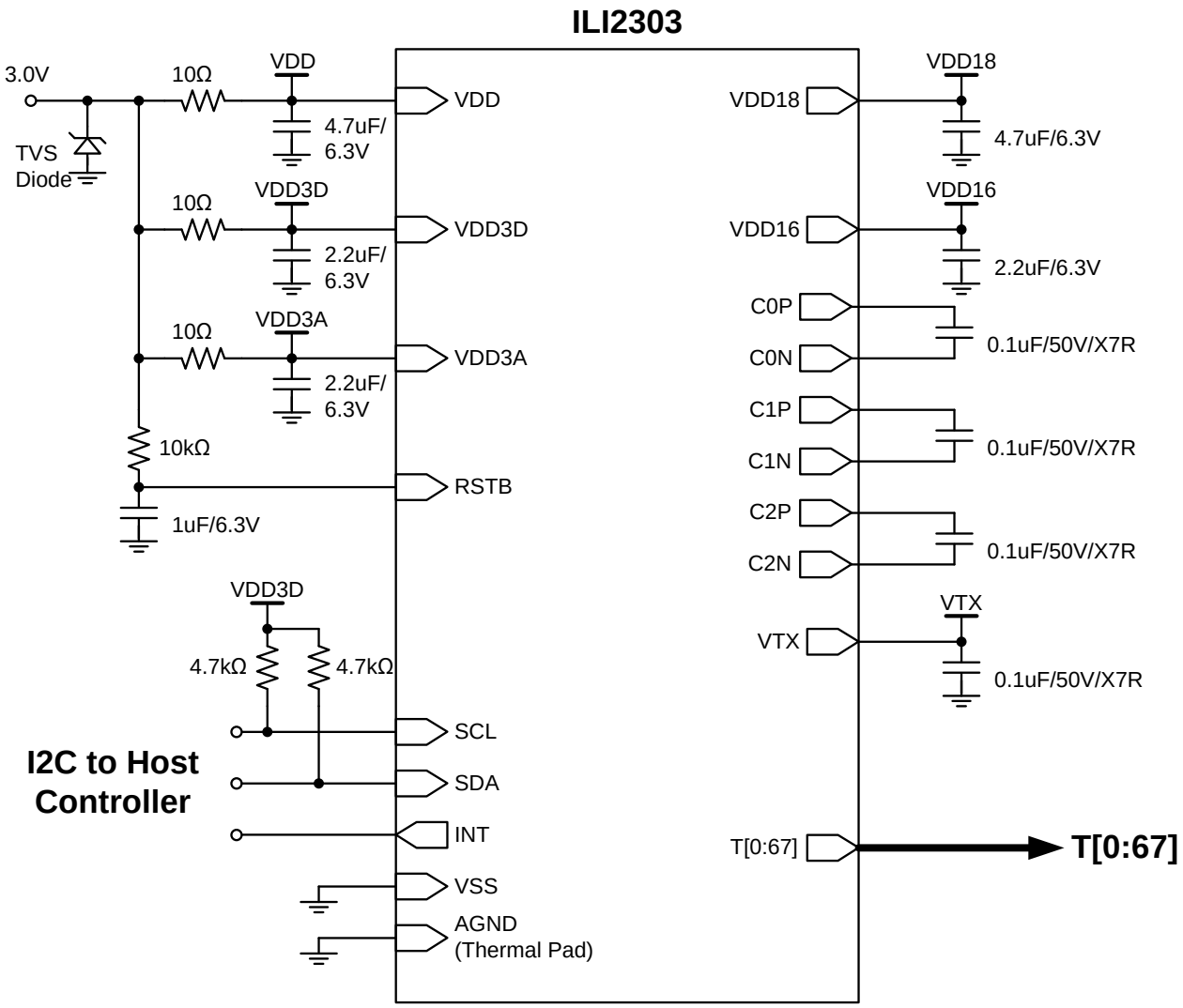


Figure 7-1: ILI2303 Typical Application Circuit