DATA SHEET

旭曜科技
ORISE TECH

OTA5182A

System-On-Chip for small size TFT-LCDs

Preliminary

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Version 0.5

Table of Contents

PAGE

SYSTEM-ON-CHIP FOR SMALL SIZE TFT-LCDS

1. GENERAL DESCRIPTION

The OTA5182A is a single chip solution dedicated to small size color TFT-LCDs. It combines on the same substrate a source driver, a gate driver, a timing controller and a power supply circuit. The system can be configured either through a 3-wire serial interface or through several individual control pins.

The 480-output channels source driver have 6-bit resolution or 8-bit if the dithering technique function is selected. The gamma correction is implemented with a resistor ladder.

The timing controller supports 4 different timings suitable for small size color TFT panels with PAL and NTSC.

A charge pump generates from a single power supply all powers supplies of the system such as analog voltage for source driver or high/low voltage of the gate driver. Finally, a general purpose DCDC PWM controller is also included.

2. FEATURES

- LCD driver with timing controller
- Supports resolution: 480x240
- 480 source output channels
- 242 gate output channels
- 8-bit resolution 256 gray scale wit Dithering
- 128 gray scales with contrast and brightness control
- Supports Raw Data and Serial RGB mode and CCIR656
- Display control and function optioned by 3-wire serial communication control
- Maximum operating frequency: 27MHz (max)
- Built-in DC-DC control circuit, charge pump circuit, VCOM circuit (AC adjustment through 3-wire program)
- Built-in R-DAC gamma correction (can be adjusted by three gamma buffers)
- Output deviation: +-35mV (max)
- Power for Digital interface VDDIO: 1.8V~3.6V
- Power for Pump Source: 3.0V ~ 3.6V
- COG with poly-imide
- Line Inversion
- Built-in power saving mode

3. ORDERING INFORMATION

Product Number	Package Type
OTA5182A-C	Chip Form with Gold Bump

4. BLOCK DIAGRAM

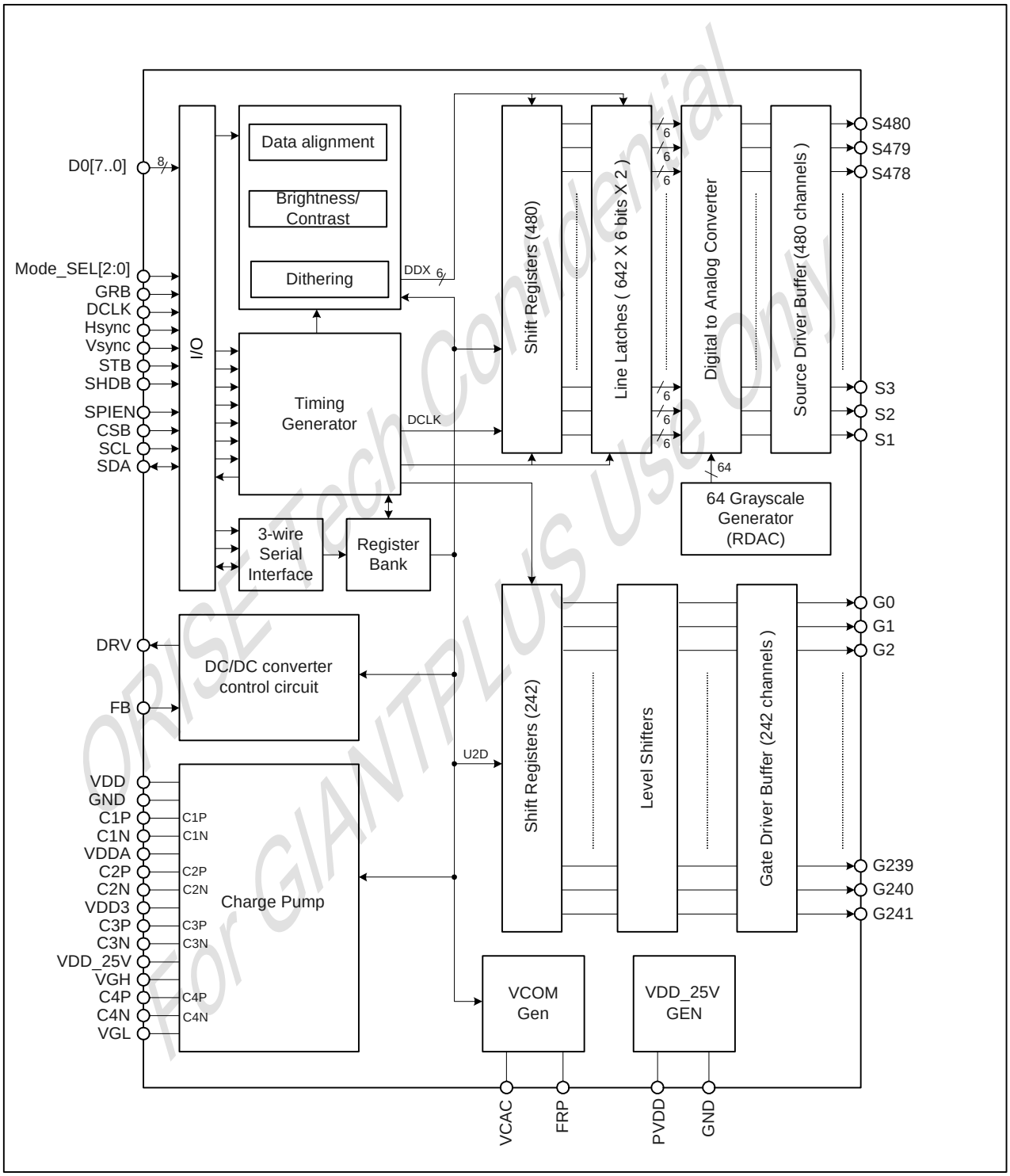


Figure 1: OTA5182A block diagram

5. SIGNAL DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
SERIAL COMMUNICATION INTERFACE		
SCL	I	Serial communication clock input.
CSB	I	Serial communication chip select.
SDA	I	Serial communication data input.
TIMING CONTROLLER (TCON)		
DCLK	I	Clock signal. Data are latched onto the Line Latch on the positive edge of DCLK.
HSYNC	I	Horizontal sync input. Negative polarity.
VSYNC	I	Vertical sync input. Negative polarity.
STB	I	Standby mode (active low). STB = "L": T-CON, source driver and DC-DC converter are off. All outputs are High-Z. STB = "H" Normal operation. (**Default setting)**
GRB	I	Global reset pin (active low). GRB = "L": The controller is reset; charge pump and DCDC are off. Bypass Serial Settings. GRB = "H": Global Reset controlled by serial register GRB. (**Default setting)**
D0[7..0]	I	Data input (DIN). 8-bit color sub-pixel (R, G or B). D07: MSB; D00: LSB.
SOURCE DRIVER		
S1~S480	O	Source driver output signals.
GATE DRIVER		
G0~G241	O	Gate driver output signals.
VCOM GENERATOR		
FRP	O	Frame polarity output. This signal is toggling between VCAC and GND.
VCAC	PO	Defines the amplitude of the VCOM swing (VCOM_AC value).
VCOMDC	O	VCOM DC level output.
POWER SUPPLY		
VDD	P	Charge Pump power supply.
VDD_25V	PO	Digital power supply.
VDDIO	P	Input I/O power supply
GND	P	Digital ground.
AGND	P	Analog ground for source driver.
VDDA	PO	Intermediate voltage for Charge Pump.
VDD3	PO	Intermediate voltage for Charge Pump.
VGH	PO	Positive power supply for gate driver outputs: +18V
VGL	PO	Negative Low power supply for gate driver outputs: -6V
C1P/N C2P/N C3P/N C4P/N	C	Pins to connect capacitors for power circuitry.
DC TO DC CONVERTER		
DRV	O	Gate signal for the power transistor of the boost converter.
FB	I	Main boost regulator feedback input.

SYMBOL	TYPE	DESCRIPTION
		Connect feedback resistive divider to GND. FB threshold is 0.6V nominal.
FB_P	I	ILED input for driving one LED application
FB_N	O	ILED output for driving one LED application
OTHER		
T_IN[23:1]	T	Test pins for OriseTech internal testing only. User should leave it open.
T_OUT[21:1]	T	Test pins for OriseTech internal testing only. User should leave it open.
DUM_VDD	D	Dummy pin for shielding, internally connected to VDD. User should leave it open.
DUMMY	D	Dummy pin, internally connected to GND. User should leave it open.
COM1	S	Internal left pass line for COM signal between input and output pins
COM2	S	Internal right pass line for COM signal between input and output pins
P_SET[1:0]	I	Internal power setting control P_SET1 = "Low" P_SET0 = "Low" (Default setting) User should leave P_SET0 open or connect it to Low. P_SET1 ="High": Reserved for future requirement.
ALIGN mark	M	For assembly alignment.

Type I: input, O: output, I/O: input/output, P: power (in), PO: power out, D: dummy, S: short pin, T: test pin, M: mark, C: capacitor pin

6. FUNCTIONAL DESCRIPTIONS

6.1. Register Bank

There is a total of 16 registers each containing several parameters. For a detailed description of the parameters refer to Table 1.

The serial register has read/write function. D[15:12] are the register address, D[11] defined the read or write mode and D[10:0] are the data.

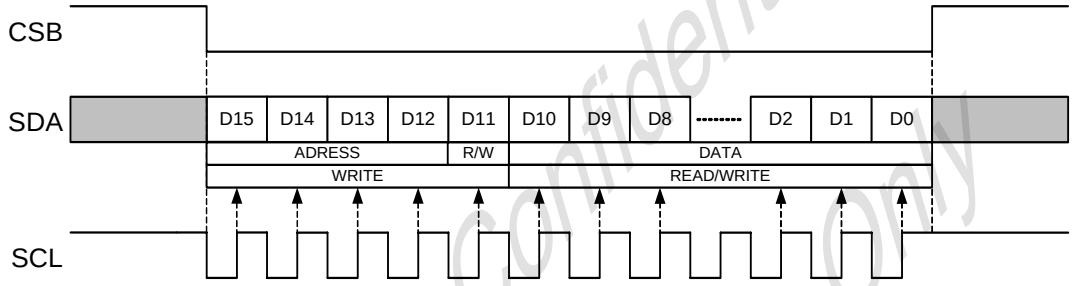


Figure 2: Serial Interface read/write sequence

At power-on, the default values specified for each parameter (in Table 1) are taken.

All data, except S0 D[3:2], are validated on the negative edge of Vsync.

In 3-wire register, GRB clear registers to default value except GRB value.

If less than 16-bit data are read during the CS low time period the data is cancelled.

6.2. Register summary

Table 1: Serial register table

Reg	ADRESS				CONTENT											
N°	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
S0	0	0	0	0	R/W	-	-	-	-				GRB (1)	STB (1)	SHDB (0)	SHCB (1)
S1	0	0	0	1	R/W	-	-	-	GAMAH (000)			PDTY (00)		FBV (100)		
S2	0	0	1	0	R/W	-	-				000			DITHB (0)	PFON (0)	1
S3	0	0	1	1	R/W	-	-	-	-	0	0	0	CONST (1000)			
S4	0	1	0	0	R/W	-	-	-	-	-			FPOL (0)	0	UD (1)	SHL (1)
S5	0	1	0	1	R/W	-				VDC EN(0)	VCOMDC (100000)					
S6	0	1	1	0	R/W	-	-	-	-	-		PALM (0)	PAL (0)	SEL (000)		
S7	0	1	1	1	R/W	-	-	-	-	BRADJ (1000000)						
S8	1	0	0	0	R/W	-	-					DDL (00000)				
S10	1	0	1	0	R/W	-	-	-	-	-	FRAD (00)		HDL (0000)			
S12	1	1	0	0	R/W	-	-	-	-					VCSL (101)		
S14	1	1	1	0	R/W	-	-	-				GAMSEL(0)	0	0	1	1

Note: Gray register are reserved registers.

6.3. Register description

6.3.1. S0: System settings

Adress	Bit	Description		Default
0000	[3:0]	Bit3(GRB)	Global reset.	xxxx_1101b
		Bit2(STB)	Standby mode setting.	
		Bit1(SHDB)	DC-DC converter shutdown setting.	
		Bit0(SHCB)	Charge Pump shutdown setting.	

Bit3	GRB function
0	The controller is resets, the charge pump and DCDC is off. Reset all register to default value.
1	Normal operation. (default)

Bit2	STB function
0	T-CON, source driver and DC-DC converter are off. All outputs are High-Z.
1	Normal operation. (default)

Bit1	SHDB function
0	DC-DC converter is off. (default)
1	DC-DC converter is on. DC-DC controls by STB and power on/off sequence.

Bit0	SHCB function
0	Charge Pump converter is off.
1	Charge Pump converter is on. (default) Charge Pump controls by STB and power on/off sequence.

6.3.2. S1 settings

Adress	Bit	Description		Default
0001	[7:0]	Bit[7:5](GAMAH)	Internal GAMAH voltage generator setting for Gamma	0000_0100b
		Bit[4:3](PDTY)	PWM1 duty control for DC2DC converter	
		Bit[2:0](FBV)	FB1 reference level adjustment for DC2DC converter	

Bit[7:5]	GAMAH Level	unit
000	4.6	V
001	4.3	
010	4.4	
011	4.5	
100	4.7	
101	4.8	
110	4.9	
111	5.0	

Bit[4:3]	PTDY Duty	unit
00	75	%
01	55	
10	60	
11	65	

Bit[2:0]	FB Vref Level	unit
000	0.4	V
001	0.45	
010	0.5	
011	0.55	
100	0.6	
101	0.65	
110	0.7	
111	0.75	

6.3.3. S2 setting

Adress	Bit	Description		Default
0010	[5:0]	Bit2(DITH)	Dithering algorithm selection.	xx00_0001b

Bit2	DITHB function
0	Dithering on. 8-bit resolution. (default)
1	Dithering off. 6-bit resolution (last 2 bits of input data truncated).

Bit1	PFON function
0	PFON="L", Pre-filter off
1	PFON="H", Pre-filter on Remark: Disable this function In RAW DATA MODE mode

6.3.4. S3 settings

Adress	Bit	Description		Default
0011	[3:0]	Bit[3:0](CONST)	RGB constant level adjustment.(0.125/Step)_	x000_1000b

Bit[3:0]	RGB constrast
0x0	0
0x8	1.00
0xF	1.875

6.3.5. S4 settings

Adress	Bit	Description		Default
0100	[3:0]	Bit3 (FPOL)	FRP source driver polarity inversion polarity inversion selection.	xxxx_0011b
		Bit1 (UD)	Vertical shift direction selection.	
		Bit0(SHL)	Horizontal shift direction selection.	

Bit3	FPOL function
0	FRP=0 when positive polarity FRP=1 when negative polarity (default)
1	FRP=1 when positive polarity FRP=0 when negative polarity

Bit1	UD function
0	Scan down: First line=G241 → G240 → … → G1 → Last line=G0.
1	Scan up: First line=G0→ G1 →…→ G240 → Last line=G241. (default)

Bit0	SHL function
0	Shift left; First data=S480 → S479 → …→ S2 → Last data=S1.
1	Shift right: First data=S1→ S2 → …→ S479→ Last data=S480. (default)

6.3.6. S5 settings

Adress	Bit	Description		Default
0101	[6:0]	Bit6(VDCEN)	Setting FRP output to add DC level	X010_0000b
		Bit[5:0](VCOMDC)	VCOM DC Level adjustment	

Bit6	VDCEN function
0	VDCEN="L", without VCOM DC Level
1	VDCEN="H", with VCOM DC Level.

Bit[5:0]	VCOMDC Setting Table	unit
0x0	0.192	V
0x20	0.704	
0x3F	1.2	

6.3.7. S6 settings

Adress	Bit	Description		Default
0110	[4:0]	Bit4(PALM)	Select skip method in PAL mode interface	xxx0_0000b
		Bit3(PAL)	PAL/NTSC selection.	
		Bit[2:0](SEL)	Select Raw data/SERIAL RGB MODE path and input data format When SEL[2:0] select different, AC timing also different.	

Bit4	PALM function
0	PAL 280 active lines. **(default)**
1	PAL 288 active lines.

Bit3	PAL function
0	NTSC Input format (240 active line). (default)
1	PAL Input format.

Bit[2:0]	SEL function	Operating Frequency
000	Select RAW DATA MODE path, special data format(DDX) input.	9.7MHz
001	Select SERIAL MODE path, normal data format(DIN) input	24.54MHz
010	Select SERIAL MODE path, normal data format(DIN) input.	27MHz
111	Select CCIR_656 path, format(YcbCr) input.	27MHz

6.3.8. S7 settings

Adress	Bit	Description		Default
0111	[6:0]	Bit[6:0](BRADJ)	Brightness Level Adjustment	x100_0000b

Bit[6:0]	Brightness level
0x00	-256
0x40	0
0x7F	+252

6.3.9. S8 settings

Adress	Bit	Description		Default
1000	[4:0]	Bit[4:0](DDL)	Horizontal Data start delay selection.	xxx0_0000b

Bit[4:0]	DDL function	
	NO.	unit
00000	0	DCLK
00001	+1	
00010	+2	
00011	+3	
00100	+4	
00101	+5	
00110	+6	
00111	+7	
01000	+8	
01001	+9	
01010	+10	
01011	+11	
01100	+12	
01101	+13	
01110	+14	
01111	+15	
10000	-1	
10001	-2	
10010	-3	
10011	-4	
10100	-5	
10101	-6	
10110	-7	
10111	-8	
11000	-9	
11001	-10	
11010	-11	
11011	-12	
11100	-13	
11101	-14	
11110	-15	
11111	-16	

6.3.10. S10 setting

Adress	Bit	Description		Default
1010	[5:0]	Bit[5:4](FRAD)	Odd frame or Even frame advance select.	xx00_0000b
		Bit[3:0](HDL)	Vertical Data start delay selection.	

Bit[5:4]	FRAD function
00	Odd/Even frame Tstv are the same
01	Even frame Tstv=HDL setting+1, unit=H
10	ODD frame Tstv=HDL setting+1, unit=H **Remark: This function is enable in SEL[2:0]="111" mode**

Bit[3:0]	HDL function

Bit3	Bit2	Bit1	Bit0	NO.
0	0	0	0	0(default)
0	0	0	1	+1
0	0	1	0	+2
0	0	1	1	+3
0	1	0	0	+4
0	1	0	1	+5
0	1	1	0	+6
0	1	1	1	+7
1	0	0	0	+8
1	0	0	1	-1
1	0	1	0	-2
1	0	1	1	-3
1	1	0	0	-4
1	1	0	1	-5
1	1	1	0	-6
1	1	1	1	-7

6.3.11. S12 setting

Adress	Bit	Description		Default
1100	[2:0]	Bit[2:0](VCSL)	VCAC Level Selection	xxxx_x101b

Bit[2:0]	VCAC Level	unit
000	4.5	V
001	4.6	
010	4.7	
011	4.8	
100	4.9	
101	5.0	
110	5.1	
111	5.2	

6.3.12. S14 settings

Adress	Bit	Description		Default
1110	[4:0]	Bit4(GAMSEL)	Gamma R Table selection	xxx0_0011b

Bit4	GAMSEL function
0	GAMSEL="L" select GAM1 value
1	GAMSEL="H" select GAM2 value

6.4. Power on/off sequence

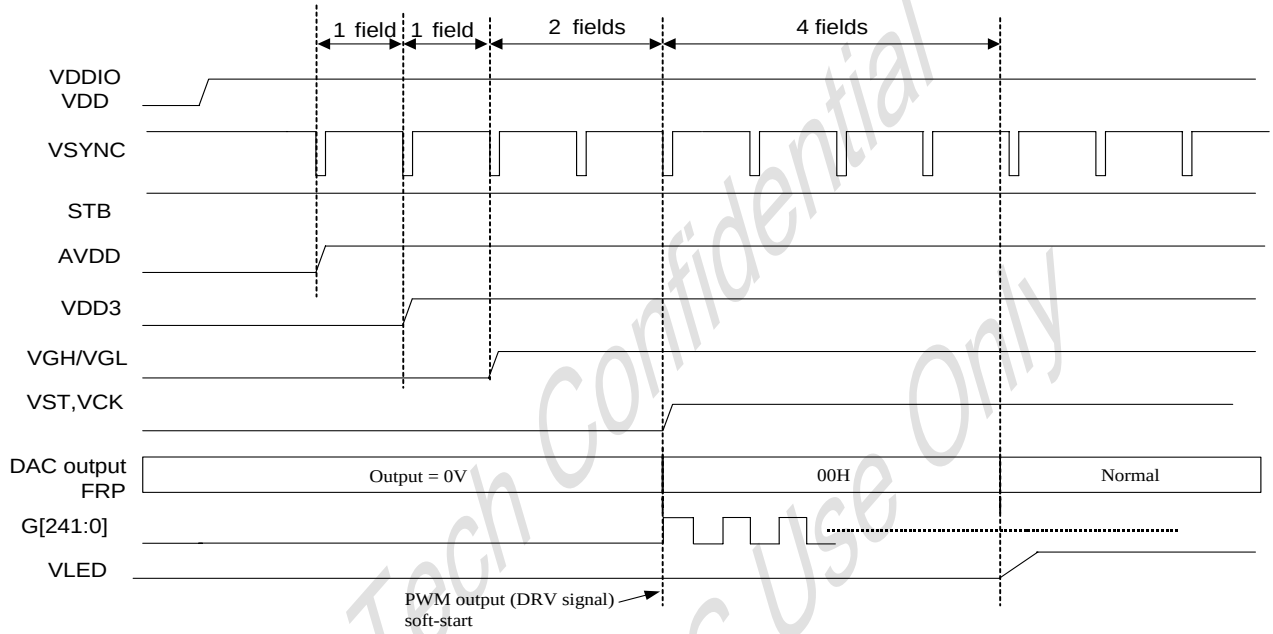


Figure 3: Power on sequence

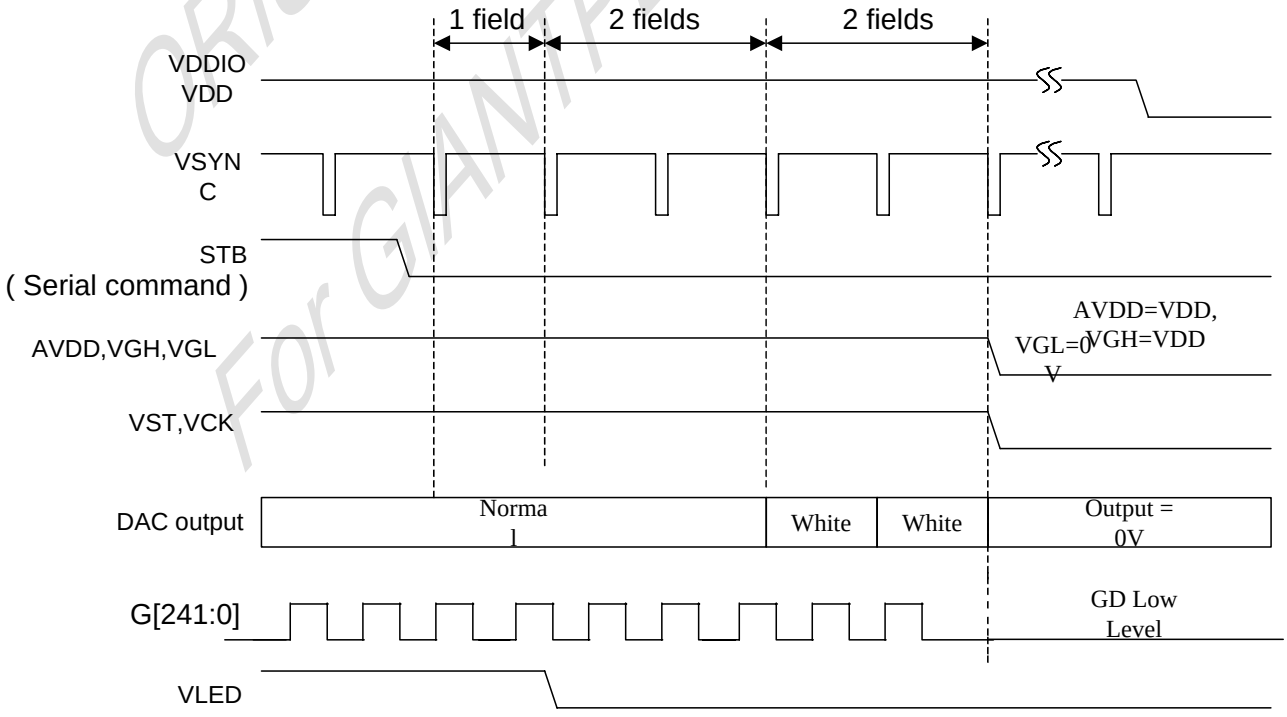


Figure 4: Power off sequence

6.5. Relationship between SD input data and output voltages

The figure below shows the relationship between the input data and the output voltage. Please refer to the following pages to get the relative resistor value and voltage calculation method. Please note the gamma tables may vary for each customer.

GAM1(GAMSEL=0)					GAM2(GAMSEL=1)				
Data	COM=L		COM=H		Data	COM=L		COM=H	
00H	GAMAH *	0.990	GAMAH *	0.040	00H	GAMAH *	1	GAMAH *	0.04
01H	GAMAH *	0.890	GAMAH *	0.140	01H	GAMAH *	0.962	GAMAH *	0.078
02H	GAMAH *	0.794	GAMAH *	0.236	02H	GAMAH *	0.929	GAMAH *	0.111
03H	GAMAH *	0.762	GAMAH *	0.268	03H	GAMAH *	0.9	GAMAH *	0.14
04H	GAMAH *	0.737	GAMAH *	0.293	04H	GAMAH *	0.872	GAMAH *	0.168
05H	GAMAH *	0.712	GAMAH *	0.318	05H	GAMAH *	0.846	GAMAH *	0.194
06H	GAMAH *	0.694	GAMAH *	0.336	06H	GAMAH *	0.82	GAMAH *	0.22
07H	GAMAH *	0.677	GAMAH *	0.353	07H	GAMAH *	0.794	GAMAH *	0.246
08H	GAMAH *	0.662	GAMAH *	0.368	08H	GAMAH *	0.768	GAMAH *	0.272
09H	GAMAH *	0.647	GAMAH *	0.383	09H	GAMAH *	0.747	GAMAH *	0.293
10H	GAMAH *	0.634	GAMAH *	0.397	10H	GAMAH *	0.726	GAMAH *	0.314
11H	GAMAH *	0.620	GAMAH *	0.410	11H	GAMAH *	0.705	GAMAH *	0.335
12H	GAMAH *	0.608	GAMAH *	0.422	12H	GAMAH *	0.684	GAMAH *	0.356
13H	GAMAH *	0.596	GAMAH *	0.434	13H	GAMAH *	0.663	GAMAH *	0.377
14H	GAMAH *	0.586	GAMAH *	0.444	14H	GAMAH *	0.642	GAMAH *	0.398
15H	GAMAH *	0.576	GAMAH *	0.454	15H	GAMAH *	0.621	GAMAH *	0.419
16H	GAMAH *	0.567	GAMAH *	0.463	16H	GAMAH *	0.6	GAMAH *	0.44
17H	GAMAH *	0.558	GAMAH *	0.472	17H	GAMAH *	0.586	GAMAH *	0.454
18H	GAMAH *	0.550	GAMAH *	0.480	18H	GAMAH *	0.572	GAMAH *	0.468
19H	GAMAH *	0.543	GAMAH *	0.487	19H	GAMAH *	0.558	GAMAH *	0.482
20H	GAMAH *	0.535	GAMAH *	0.495	20H	GAMAH *	0.545	GAMAH *	0.495
21H	GAMAH *	0.528	GAMAH *	0.502	21H	GAMAH *	0.534	GAMAH *	0.506
22H	GAMAH *	0.521	GAMAH *	0.508	22H	GAMAH *	0.524	GAMAH *	0.516
23H	GAMAH *	0.514	GAMAH *	0.514	23H	GAMAH *	0.513	GAMAH *	0.527
24H	GAMAH *	0.508	GAMAH *	0.520	24H	GAMAH *	0.503	GAMAH *	0.537
25H	GAMAH *	0.503	GAMAH *	0.525	25H	GAMAH *	0.492	GAMAH *	0.548
26H	GAMAH *	0.497	GAMAH *	0.531	26H	GAMAH *	0.484	GAMAH *	0.556
27H	GAMAH *	0.491	GAMAH *	0.536	27H	GAMAH *	0.475	GAMAH *	0.565
28H	GAMAH *	0.485	GAMAH *	0.542	28H	GAMAH *	0.467	GAMAH *	0.573
29H	GAMAH *	0.479	GAMAH *	0.547	29H	GAMAH *	0.459	GAMAH *	0.581
30H	GAMAH *	0.473	GAMAH *	0.552	30H	GAMAH *	0.45	GAMAH *	0.59
31H	GAMAH *	0.468	GAMAH *	0.557	31H	GAMAH *	0.442	GAMAH *	0.598
32H	GAMAH *	0.462	GAMAH *	0.563	32H	GAMAH *	0.433	GAMAH *	0.607
33H	GAMAH *	0.457	GAMAH *	0.567	33H	GAMAH *	0.425	GAMAH *	0.615
34H	GAMAH *	0.452	GAMAH *	0.572	34H	GAMAH *	0.417	GAMAH *	0.623
35H	GAMAH *	0.447	GAMAH *	0.576	35H	GAMAH *	0.408	GAMAH *	0.632
36H	GAMAH *	0.442	GAMAH *	0.581	36H	GAMAH *	0.4	GAMAH *	0.64
37H	GAMAH *	0.437	GAMAH *	0.586	37H	GAMAH *	0.392	GAMAH *	0.648
38H	GAMAH *	0.432	GAMAH *	0.591	38H	GAMAH *	0.385	GAMAH *	0.655
39H	GAMAH *	0.426	GAMAH *	0.596	39H	GAMAH *	0.377	GAMAH *	0.663
40H	GAMAH *	0.421	GAMAH *	0.600	40H	GAMAH *	0.369	GAMAH *	0.671
41H	GAMAH *	0.416	GAMAH *	0.605	41H	GAMAH *	0.362	GAMAH *	0.678
42H	GAMAH *	0.411	GAMAH *	0.610	42H	GAMAH *	0.354	GAMAH *	0.686
43H	GAMAH *	0.405	GAMAH *	0.615	43H	GAMAH *	0.346	GAMAH *	0.694
44H	GAMAH *	0.401	GAMAH *	0.620	44H	GAMAH *	0.339	GAMAH *	0.701
45H	GAMAH *	0.397	GAMAH *	0.625	45H	GAMAH *	0.331	GAMAH *	0.709
46H	GAMAH *	0.392	GAMAH *	0.631	46H	GAMAH *	0.323	GAMAH *	0.717
47H	GAMAH *	0.387	GAMAH *	0.636	47H	GAMAH *	0.316	GAMAH *	0.724
48H	GAMAH *	0.382	GAMAH *	0.642	48H	GAMAH *	0.308	GAMAH *	0.732
49H	GAMAH *	0.377	GAMAH *	0.648	49H	GAMAH *	0.298	GAMAH *	0.742
50H	GAMAH *	0.372	GAMAH *	0.654	50H	GAMAH *	0.289	GAMAH *	0.751
51H	GAMAH *	0.367	GAMAH *	0.660	51H	GAMAH *	0.279	GAMAH *	0.761
52H	GAMAH *	0.361	GAMAH *	0.666	52H	GAMAH *	0.269	GAMAH *	0.771
53H	GAMAH *	0.355	GAMAH *	0.673	53H	GAMAH *	0.259	GAMAH *	0.781
54H	GAMAH *	0.349	GAMAH *	0.680	54H	GAMAH *	0.25	GAMAH *	0.79
55H	GAMAH *	0.342	GAMAH *	0.688	55H	GAMAH *	0.24	GAMAH *	0.8
56H	GAMAH *	0.334	GAMAH *	0.696	56H	GAMAH *	0.229	GAMAH *	0.811
57H	GAMAH *	0.326	GAMAH *	0.705	57H	GAMAH *	0.219	GAMAH *	0.821
58H	GAMAH *	0.318	GAMAH *	0.715	58H	GAMAH *	0.204	GAMAH *	0.836
59H	GAMAH *	0.308	GAMAH *	0.726	59H	GAMAH *	0.19	GAMAH *	0.85
60H	GAMAH *	0.295	GAMAH *	0.740	60H	GAMAH *	0.176	GAMAH *	0.864
61H	GAMAH *	0.279	GAMAH *	0.757	61H	GAMAH *	0.137	GAMAH *	0.903
62H	GAMAH *	0.250	GAMAH *	0.790	62H	GAMAH *	0.092	GAMAH *	0.948
63H	GAMAH *	0.090	GAMAH *	0.940	63H	GAMAH *	0.04	GAMAH *	1

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute maximum ratings

Table 2: Absolute maximum ratings

Parameter	Symbol	Unit	Rating	Note
Logic supply	VDDIO	V	-0.5 to +6	
Analog supply	VDDA	V	-0.5 to +6	
Power supply	VDD	V	-0.5 to +6	
Input Voltage	Others	V	-0.3 to VDDIO+0.3	
Output Voltage	S1~ S480	V	-0.3 to VDDA+0.3	
	Others	V	-0.3 to VDDIO+0.3	
Operating Temperature	T_{OPR}	°C	-30 to +85	
Storage Temperature	T_{STG}	°C	-55 to +100	

Note: If Ics are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

7.2. Digital DC characteristics

Table 3: Digital DC characteristics (VDD=3.3V, AGND=GND=0V, T_{OPR} = -30°C to +85°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDDIO		1.8	3.3	3.6	V
Low Level Input Voltage	Vil	Digital input pins	GND	-	0.3xVDDIO	V
High Level Input Voltage	Vih	Digital input pins	0.7xVDDIO	-	VDDIO	V
High Level Output Voltage	Voh	Q1H: Ioh = 400µA	VDDIO-0.4	-	VDDIO	V
Low Level Output Voltage	Vol	Q1H: Iol = -400µA	GND	-	GND+0.4	V
Input Leakage Current	Iil		-	-	±1.0	µA
Digital Stand-by Current	Ist	DCLK is stopped, Outputs are High-Z	-	-	100	µA
Digital Operating Current	Icc	Fclk=24.54 MHz, Fld=15KHz	-	5	7.5	mA

7.3. Analog DC characteristics

Table 4: Analog DC characteristics (VDDIO=3.3V, VDD=3.3V, AGND=GND=0V, T_{OPR} = -30°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDDA		5	5.7	6.5	V
Voltage Deviation of Outputs	Vvd	Sn=0.2V~0.5V, Sn=4.8V~4.5V	-	±20	±35	mV
		Sn = 0.5V ~ 4.5V	-	±15	±20	
Dynamic Range of Output	Vdr	S1 ~ S480	0.2	-	4.8	V
Analog Stand-by Current	Ist	STB=”0”	-	-	100	µA
Analog Operating Current	IDD	No load, line inversion, DCLK=27MHz, Th=63.5us	-	2.0	2.8	mA

7.4. Power DC characteristics

Table 5: Analog DC characteristics (VDDIO=3.3V, VDD=3.3V, AGND=GND=0V, T_{OPR} = -30°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDD		3.0	3.3	3.6	V
DRV output voltage	VDRV		0	-	VDD	V
Feed back voltage	VFB	DC/DC operating, VBL current=20mA DC_FB_LEVEL=100	0.55	0.6	0.65	V
Base drive current	IDRV	VDDIO=3 V,DRV=0.7 V	-	-	10	mA
VCOM AC voltage	$VCOM_{AC}$	Function of VCOM_AC[3..0] setting	4.5	5.0	5.2	V
Low level Output current	IOL_{FRP}	Sink current Vo=0.5V		-10	-	mA
High level Output current	IOH_{FRP}	Driving current Vo=VCAC-0.5V		-10	-	mA
Positive high-voltage power	VGH	No Load	16.5	18.5	20	V
Negative high-voltage power	VGL	No Load; function of VCOM_AC[3..0] setting.	-7	-6	-5.5	V
Power Stand-by Current	Ipst	STB="0"	-	-	100	µA
Power Operating Current	IPDD	DCLK=27MHz, Th=63.5us	-	12	14	mA

7.5. AC characteristics

Table 6: AC characteristics (VDD=3.3V, AGND=GND=0V, T_{OPR} = -30°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CLK pulse duty	Tcw		40	50	60	%
Delay between Hsync and DCLK	Thc		-	-	1.0	DCLK
Hsync width	Twh		1.0	-	-	DCLK
Hsync period	Th		60	63.56	67	us
Vsync setup time	Tvst		12	-	-	ns
Vsync hold time	Tvhd		12	-	-	ns
Hsync setup time	Thst		12	-	-	ns
Hsync hold time	Thhd		12	-	-	ns
Data set-up time	Tdsu	D00~D07 to DCLK	12	-	-	ns
Data hold time	Tdhd	D00~D07 to DCLK	12	-	-	ns
VSync to 1st gate Output	Tstv	Sel≠"111";By HDL[3..0] settings	6	13	21	Th
CCIR V to 1st gate Output	Tstv	Sel="111" NTCS (PAL=0); By HDL[3..0] settings	14	21	29	Th
CCIR V to 1st gate Output	Tstv	Sel="111" PAL=1; By HDL[3..0] settings	20	27	35	Th
SD output stable time	Tst	30mV precision; CL=6.75pF, R=3.62K	-	25	30	us
GD output delay time	Tgd	CL=17.6pF, R=1.29K	-	900	1500	ns
GD output rise and fall time	Tgst	CL=17.6pF, R=1.29K 10% to 90%	-	900	1500	ns
Serial communication						
Serial clock period	Tsck		320	-	-	ns
Serial clock duty cycle	Tscw		40	50	60	%

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial clock width low/high	Tssw		120			ns
Serial data setup time	Tist		120			ns
Serial data hold time	Tihd		120			ns
CSB setup time	Tcst		240			ns
CSB data hold time	Tchd		120			ns
Chip select distinguish	Tcd		1			us
Delay between CSB and Vsync	Tcv		1			us

7.6. Operating mode dependent AC characteristics

7.6.1. RAW DATA MODE

The below specifications apply for:

SEL2	SEL1	SEL0
0	0	0

Table 7: RAW DATA MODE 480x240 AC characteristics (VDD=3.3V, AGND=GND=0V, T_{OPR} = -30°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DCLK frequency	Fclk		-	9.7	-	MHz
DCLK period	Tcph		-	103	-	ns
Delay from Hsync to Source Output	Thso		-	56	-	DCLK
Delay from Hsync to Gate Output	Thgo		-	45	-	DCLK
Delay from Hsync to Gate Output off	Thgz		-	19	-	DCLK
Delay from Hsync to Q1H	Thq		-	39	-	DCLK
Delay from Hsync to FRP	Thf			59		DCLK
Delay from Hsync to 1st data input	Ths	Function of DDL[5..0] settings	68	100	131	DCLK
DC converter osc. Frequency	Fosc	Fclk/32	-	303.1	-	kHz

7.6.2. SERIAL RGB MODE

The below specifications apply for:

SEL2	SEL1	SEL0
0	0	1

Table 8: SERIAL MODE, AC characteristics (VDD=3.3V, AGND=GND=0V, T_{OPR} = -30°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DCLK frequency	Fclk		-	24.54/27	-	MHz
DCLK cycle time	Tcph		-	40/37	-	ns
Delay from Hsync to Source Output	Thso		-	143	-	DCLK
Delay from Hsync to Gate Output	Thgo		-	113	-	DCLK
Delay from Hsync to Gate Output off	Thgz		-	48	-	DCLK

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Delay from Hsync to Q1H	Thq		-	100	-	DCLK
Delay from Hsync to FRP	Thf			143		DCLK
Delay from Hsync to 1st data input	Ths	Function of DDL[5..0] settings	220	252	283	DCLK
DC converter osc. Frequency	Fosc	Fclk/64 = 383.4kHz / 421.9kHz	-	383.4 / 421.9	-	kHz

7.6.3. CCIR

The below specifications apply for:

SEL2	SEL1	SEL0
1	1	1

Table 9:CCIR MODE, AC characteristics (VDD=3.3V, AGND=GND=0V, T_{OPR} = -30°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DCLK frequency	Fclk		-	27	-	MHz
DCLK cycle time	Tcph		-	37	-	ns
CLK pulse duty	Tcw		40	50	60	%
Delay from EAV to Source Output	Thso		-	143	-	DCLK
Delay from EAV to Gate Output	Thgo		-	113	-	DCLK
Delay from EAV to Gate Output off	Thgz		-	48	-	DCLK
Delay from EAV to Q1H	Thq		-	100	-	DCLK
Delay from EAV to FRP	Thf			143		DCLK
Delay from EAV to 1st data input	Ths	Function of DDL[5..0] settings	241	273	304	DCLK
DC converter osc. Frequency	Fosc	Fclk/64	-	421.9	-	kHz

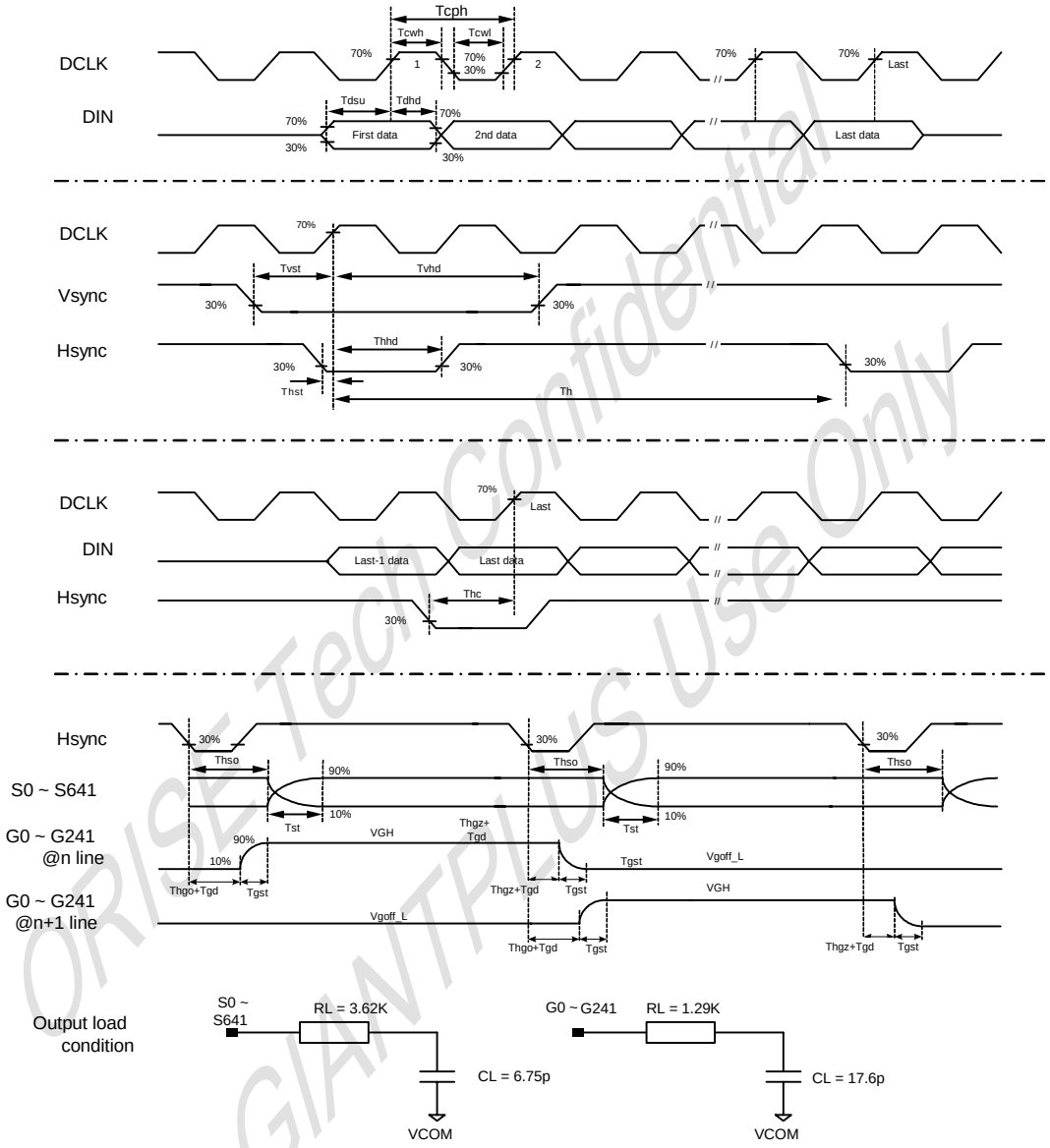


Figure 5: AC Drivers timing

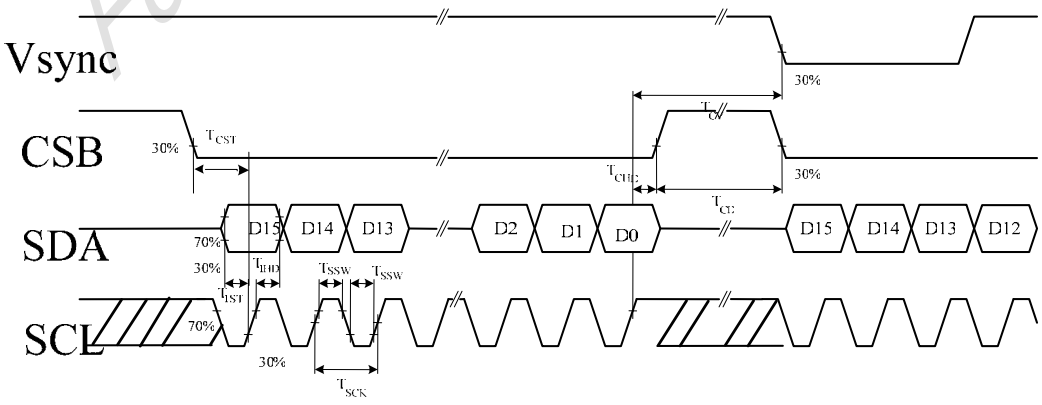
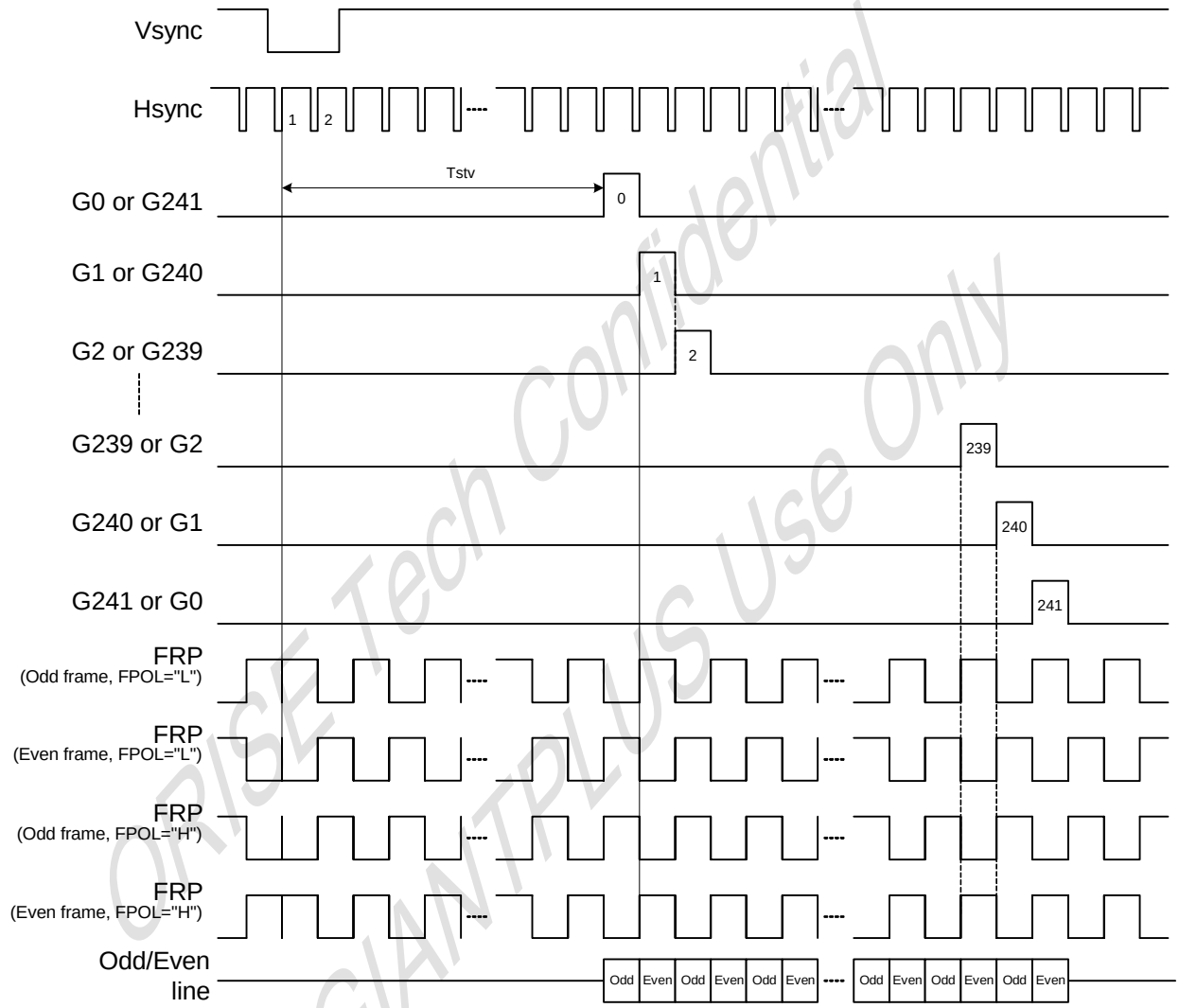


Figure 6: AC Serial communication timing



Note: SD Line 1,3,5,…, 241 =Odd line, : SD Line 2,5, 6,…, 242 =Even line

Figure 7: Vertical timing diagram

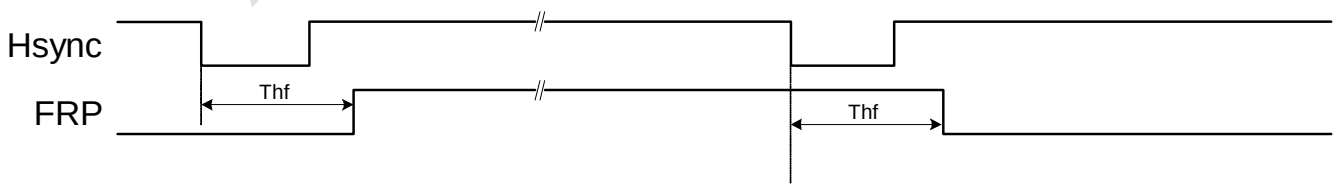


Figure 8: Horizontal timing diagram

7.7. Input Data Format

7.7.1. RAW DATA MODE

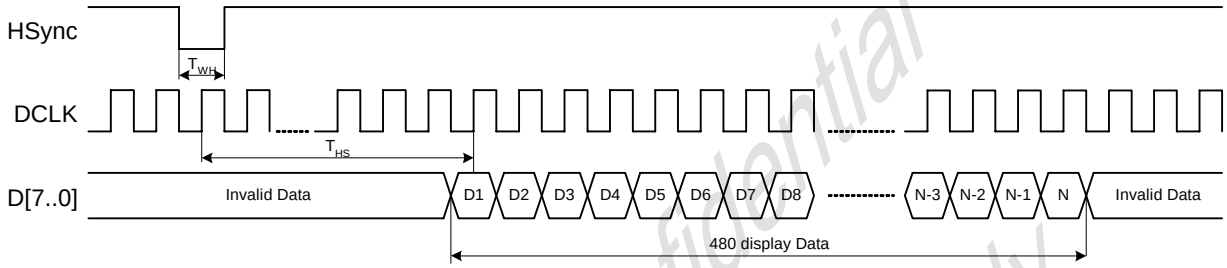


Figure 9: RAW DATA MODE data input format

7.7.2. SERIAL MODE 24.54MHz

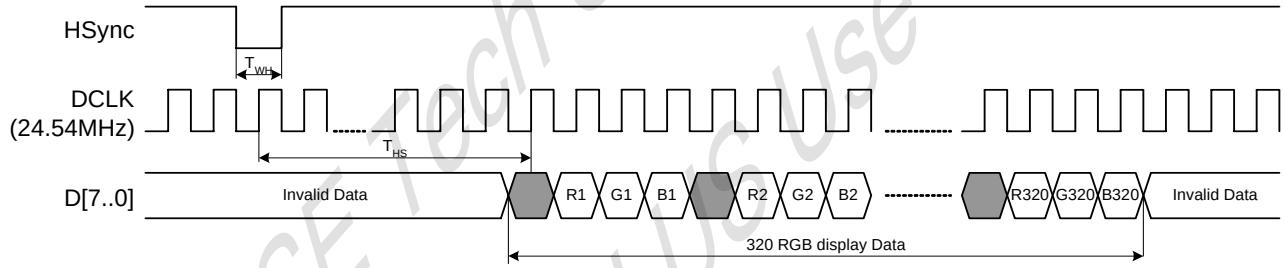


Figure 10: SERIAL MODE 24.54MHz Data input format (Sel=001)

7.7.3. SERIAL MODE 27MHz

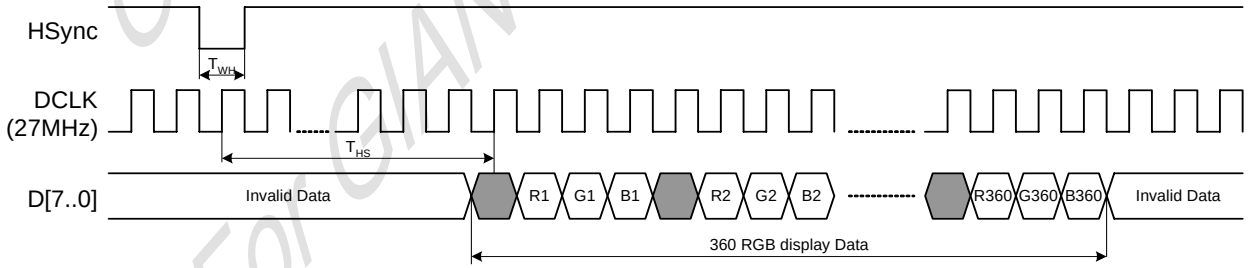


Figure 11: SERIAL MODE 27MHz Data input format (Sel=010)

7.7.4. CCIR 656

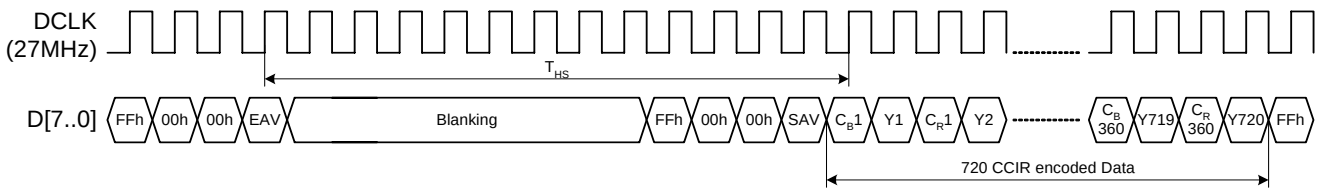


Figure 12: CCIR Data input format

7.8. Vertical input timing

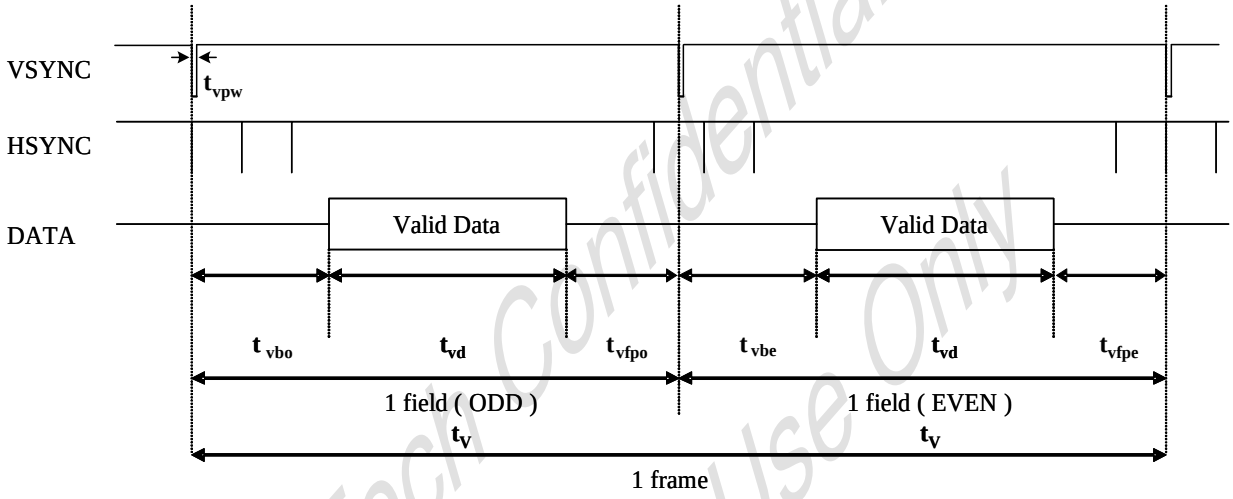


Figure 13: Vertical input timing diagram for interlace application

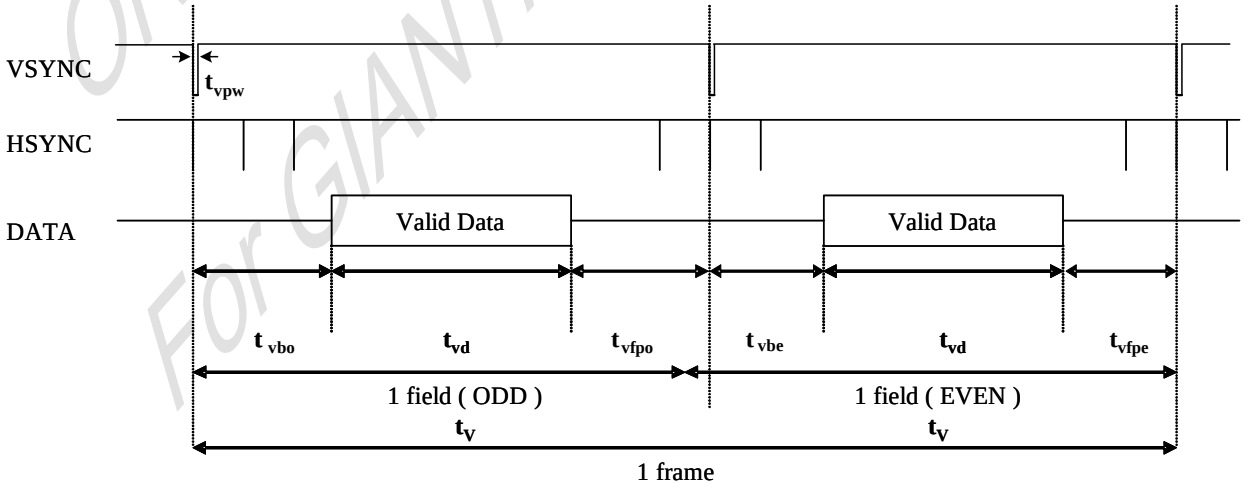


Figure 14: Vertical input timing diagram for non-interlace application

7.8.1. Raw data vertical input timing

Parameter		Symbol	Interlace			(*)Non-Interlace			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Vertical display area		t_{vd}		240			240		H
VSYNC period time		t_v	247.5	262.5	277.5	247	262	277	H
VSYNC pulse width		t_{vpw}	1 DCLK	1H	6H	1 DCLK	1H	6H	
(*)VSYNC Blanking (t_{vb})	Odd field	t_{vbo}	6	13	21	6	13	21	H
	Even field	t_{vbe}	6.5	13.5	21.5				
VSYNC Front porch (t_{vfp})	Odd field	t_{vfpo}	1.5	9.5	16.5	1	9	16	H
	Even field	t_{vfpe}	1	9	16				

7.8.2. SERIAL RGB vertical input timing

NTSC

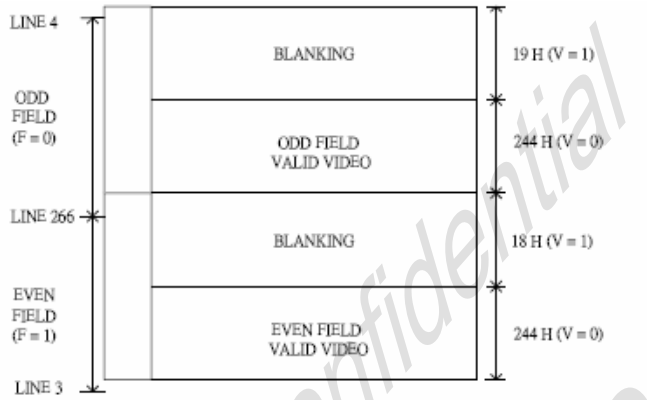
Parameter		Symbol	Interlace			(*)Non-Interlace			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Vertical display area		t_{vd}		240			240		H
VSYNC period time		t_v	247.5	262.5	277.5	247	262	277	H
VSYNC pulse width		t_{vpw}	1 DCLK	1H	6H	1 DCLK	1H	6H	
(*)VSYNC Blanking (t_{vb})	Odd field	t_{vbo}	6	13	21	6	13	21	H
	Even field	t_{vbe}	6.5	13.5	21.5				
VSYNC Front porch (t_{vfp})	Odd field	t_{vfpo}	1.5	9.5	16.5	1	9	16	H
	Even field	t_{vfpe}	1	9	16				

PAL

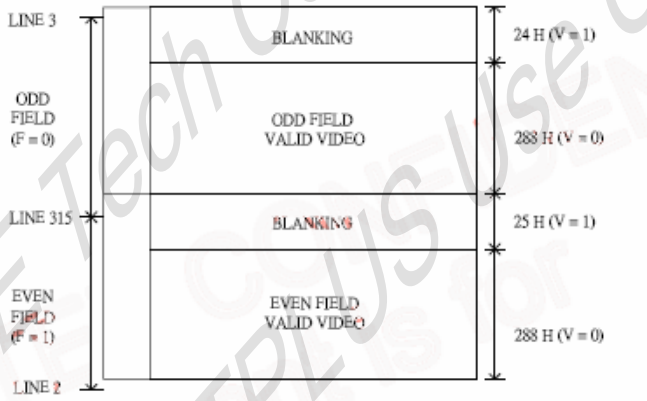
Parameter		Symbol	Interlace			(*)Non-Interlace			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Vertical display area		t_{vd}		288(280)			288(280)		H
VSYNC period time		t_v	295.5 (287.5)	312.5	325.5 (317.5)	295 (287)	312	325 (317)	H
VSYNC pulse width		t_{vpw}	1 DCLK	1H	6H	1 DCLK	1H	6H	
(*)VSYNC Blanking (t_{vb})	Odd field	t_{vbo}	6	13	21	6	13	21	H
	Even field	t_{vbe}	6.5	13.5	21.5				
VSYNC Front porch (t_{vfp})	Odd field	t_{vfpo}	1.5	11.5(19.5)	16.5	1	11(19)	16	H
	Even field	t_{vfpe}	1	11(19)	16				

(*) Non-interlace mode: NTSC is 262 lines (typical), but 263 is tolerant.

PAL is 312 lines (typical), but 313 is tolerant.



NTSC

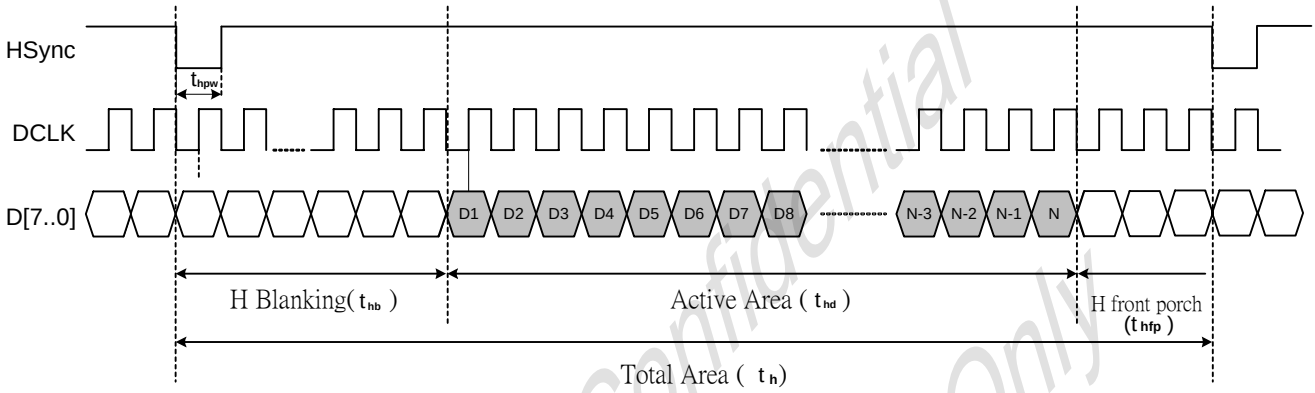


PAL

	F	H	V
1	EVEN Field	EAV	BLANKING
0	ODD Field	SAV	VALID VIDEO

Figure 15: Illustration on SERIAL RGB vertical input timing

7.9. Horizontal input timing



7.9.1. Raw Data

Parameter		Symbol	Value			Unit
Horizontal display area		t_{hd}	480			DCLK
DCLK frequency		f_{clk}	Min.	Typ.	Max	
			8.1	9.7	11.3	Mhz
1 Horizontal Line		t_h	617			DCLK
HSYNC pulse width	Min.	t_{hpw}	1			
	Typ.		1			
	Max.		96			
HSYNC blanking		t_{hb}	85	100	116	
HSYNC front porch		t_{hfp}	52	37	21	

7.9.2. SERIAL RGB MODE

NTSC

Parameter		Symbol	Value			Value			Value			Unit
Horizontal display area		t_{hd}	1280			1408			1440			DCLK
DCLK frequency		f_{clk}	Min.	Typ.	Max	Min.	Typ.	Max	Min.	Typ.	Max	
			20.47	24.54	28.66	22.5	27	31.5	22.5	27	31.5	MHz
1 Horizontal Line		t_h	1560			1716			1716			DCLK
HSYNC pulse width	Min.	t_{hpw}	1			1			1			
	Typ.		1			1			1			
	Max.		96			96			96			
HSYNC blanking		t_{hb}	237	252	268	237	252	268	237	252	268	
HSYNC front porch		t_{hfp}	43	28	12	71	56	40	39	24	8	

PAL

Parameter		Symbol	Value			Value			Unit
Horizontal display area		t_{hd}	1408			1440			DCLK
DCLK frequency		f_{clk}	Min.	Typ.	Max	Min.	Typ.	Max	
			22.5	27	31.5	22.5	27	31.5	MHz
1 Horizontal Line		t_h	1728			1728			DCLK
HSYNC pulse width	Min.	t_{hpw}	1			1			
	Typ.		1			1			
	Max.		96			96			
HSYNC blanking		t_{hb}	237	252	268	237	252	268	
HSYNC front porch		t_{hfp}	83	68	52	51	36	20	

7.9.3. 3. CCIR

Parameter		Symbol	Mode(NTSC/PAL)	Unit
Horizontal display area		t_{hd}	1440	DCLK
DCLK frequency		f_{clk}	27	MHz
1 Horizontal Line		t_h	1716	DCLK
Internal HSYNC pulse width	Min.	t_{hpw}	1	
	Typ.		1	
	Max.		-	
HSYNC blanking		t_{hb}	268	

7.10. Stand-by timing

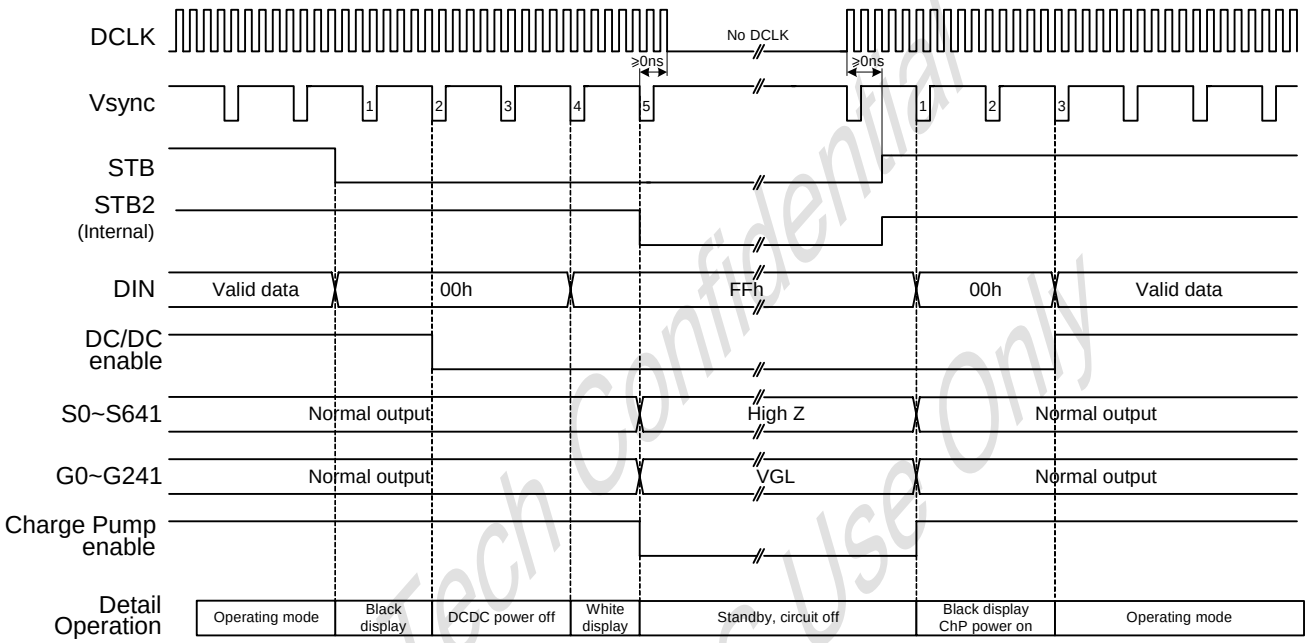


Figure 16: Stand-by timing diagram

During No DCLK, Hsync and Vsync can be stopped. But in all other cases Hsync and Vsync must be active.

8. PANEL CONFIGURATION

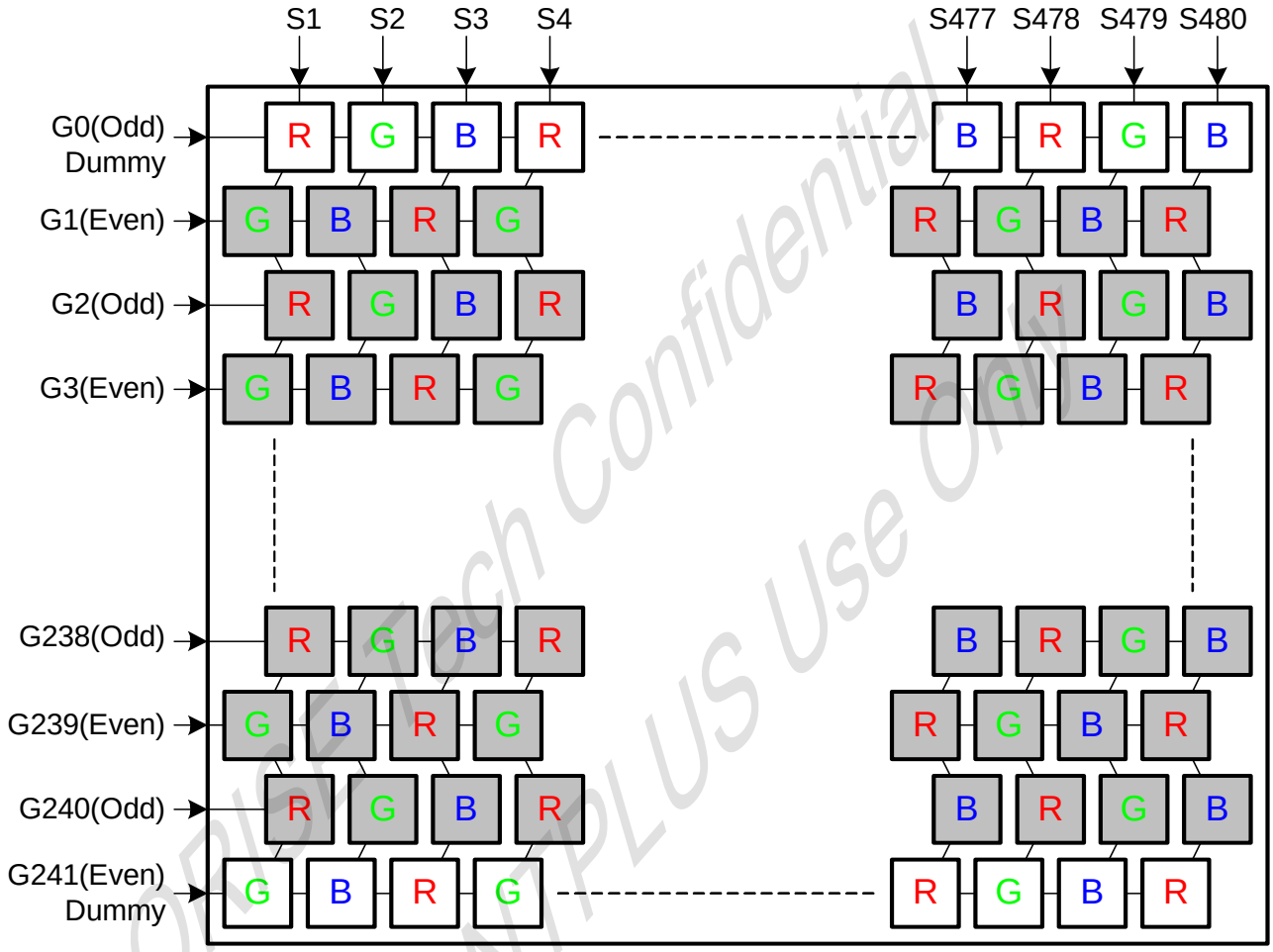
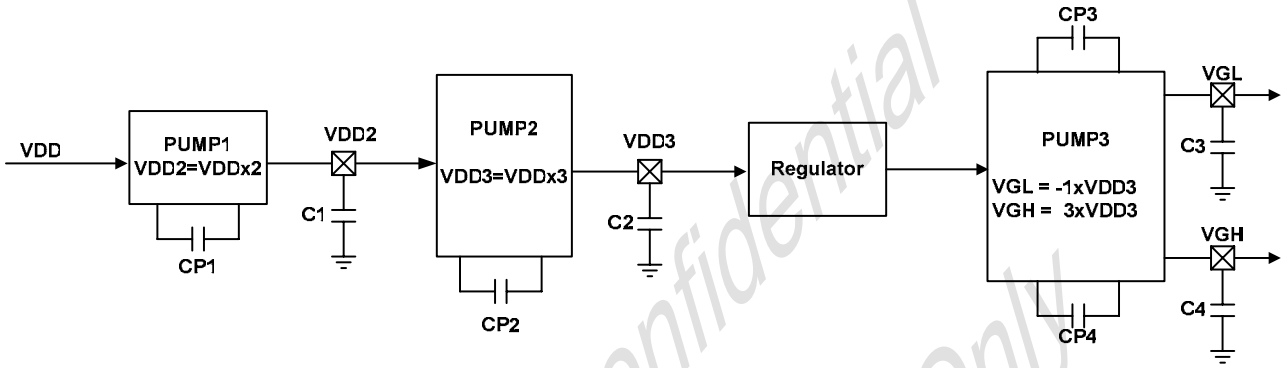


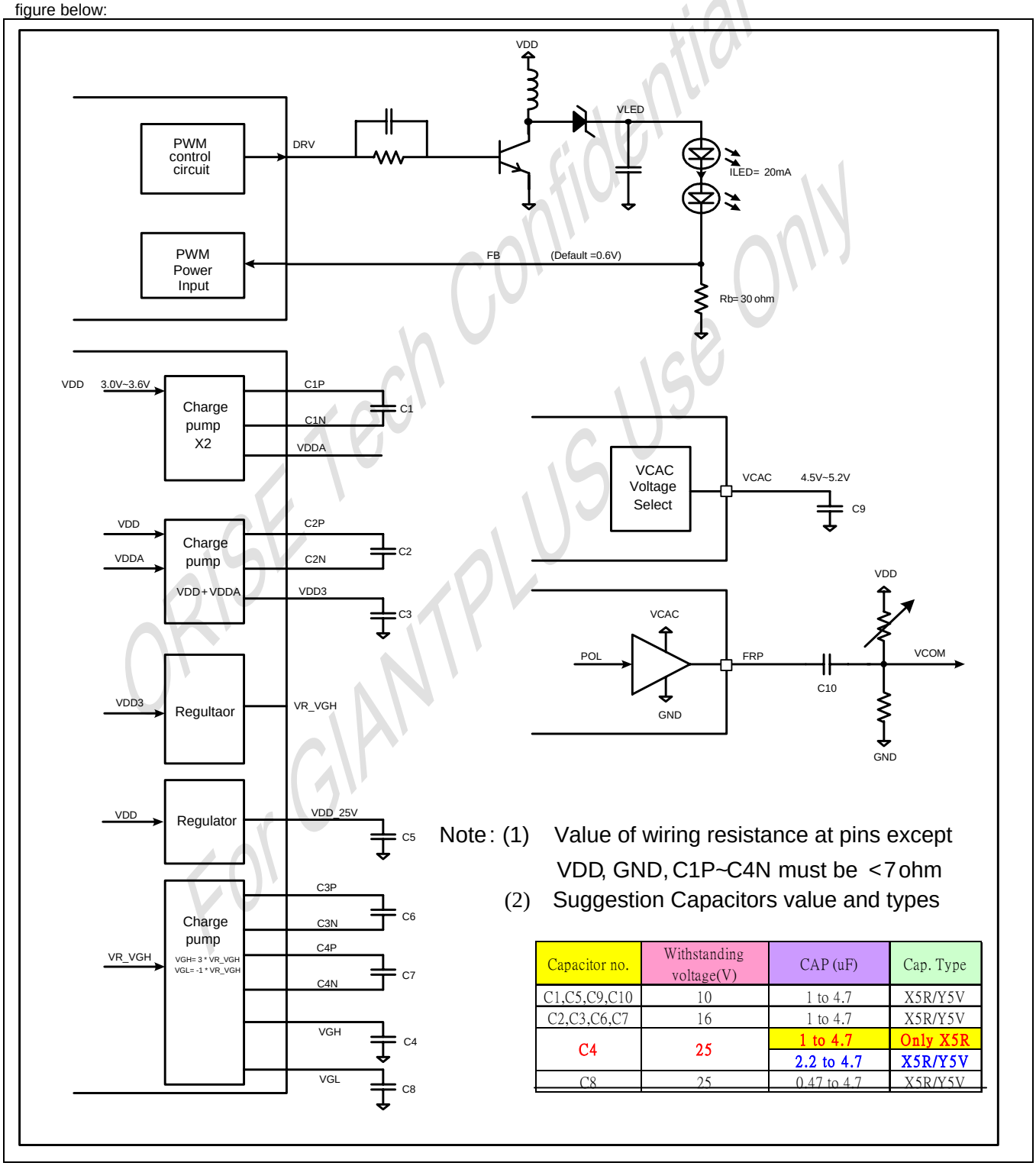
Figure 17: Delta pixel panel configuration

9. CHARGE PUMP BLOCK DIAGRAM



10. APPLICATION NOTES

The OTA5182A has a built-in power supply which generates and controls several voltages for the gate driver (VGH, VGL), for the liquid crystal common plate (VCOM, VCAC) and for the external backlight (DRV, FB, VLED). An example of typical application is shown in the figure below:



Capacitor no.	Withstanding voltage(V)	CAP (uF)	Cap. Type
C1,C5,C9,C10	10	1 to 4.7	X5R/Y5V
C2,C3,C6,C7	16	1 to 4.7	X5R/Y5V
C4	25	1 to 4.7	Only X5R
		2.2 to 4.7	X5R/Y5V
C8	25	0.47 to 4.7	X5R/Y5V

Figure 18: OTA5182A Application example

11. CHIP INFORMATION

11.1. PAD Assignment

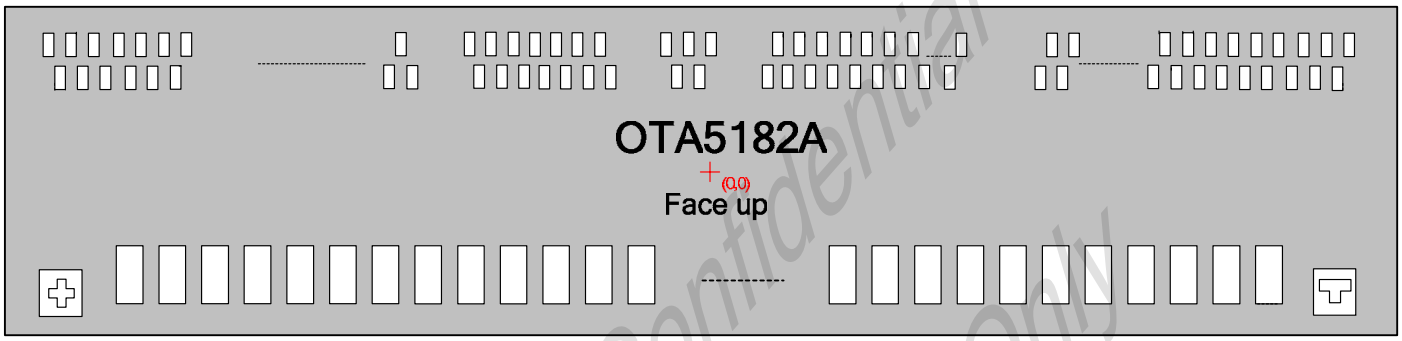


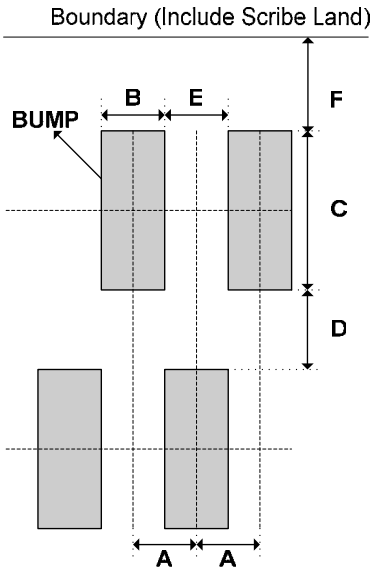
Figure 19: OTA5182A Chip Outline Dimension (Face up / included scribe line 80um)

11.2. PAD Dimension

Item	PAD No.	Size		Unit
		X	Y	
Chip Size	-	11400	670	μm
Chip thickness	-	400 ± 20		
Pad pitch	1~194	55		
	195~945	14		
Pad size	1~194	39	74	
	195~945	14	100	

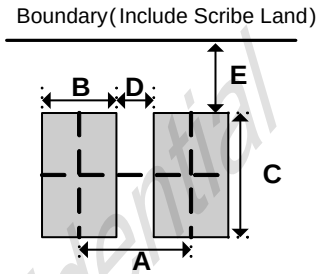
Note1: Chip size included scribe line.

11.2.1. Output Pads



Item	Sumbol	Size
Bump Pitch	A	28um
Bump Width	B	14um
Bump height	C	100um
Bump space 1	D	30um
Bump space 2	E	14um
Bump area	BxC	1400um^2
Chip boundary	F	58um

11.2.2. Input Pads



Item	Sumbol	Size
Bump Pitch	A	55um
Bump Width	B	39um
Bump height	C	74um
Bump space	D	16um
Chip boundary	E	58um
Bump area	BxC	2886um^2

11.3. Bump Characteristics

Item	Standard	Note
Bump Hardness	75Hv	± 25Hv
Bump Height	15µm	± 3µm
Co-planarity (in Chip)	R≦ 2µm	R : Max-Min
Roughness (in Bump)	R≦ 2µm	R : Max-Min
Bump Size	Long side ± 2.5µm, short side ± 2µm	
Shear Force	> 5 g/mil^2	

11.4. PAD Locations

Pad No.	Pad Name	X	Y
1	DUMMY	-5307.5	-240
2	COM1	-5252.5	-240
3	COM1	-5197.5	-240
4	VCOMDC	-5142.5	-240
5	VCOMDC	-5087.5	-240
6	VGL	-5032.5	-240
7	VGL	-4977.5	-240
8	VGL	-4922.5	-240
9	VGL	-4867.5	-240
10	C4P	-4812.5	-240
11	C4P	-4757.5	-240
12	C4P	-4702.5	-240
13	C4P	-4647.5	-240
14	C4P	-4592.5	-240
15	C4N	-4537.5	-240
16	C4N	-4482.5	-240
17	C4N	-4427.5	-240
18	C4N	-4372.5	-240
19	C4N	-4317.5	-240
20	VGH	-4262.5	-240
21	VGH	-4207.5	-240
22	VGH	-4152.5	-240
23	VGH	-4097.5	-240
24	VGH	-4042.5	-240
25	FRP	-3987.5	-240
26	FRP	-3932.5	-240
27	FRP	-3877.5	-240
28	VCAC	-3822.5	-240
29	VCAC	-3767.5	-240
30	VCAC	-3712.5	-240
31	VDD_25V	-3657.5	-240
32	VDD_25V	-3602.5	-240
33	VDD_25V	-3547.5	-240
34	VDD_25V	-3492.5	-240
35	VDD_25V	-3437.5	-240
36	VDD_25V	-3382.5	-240
37	VDD_25V	-3327.5	-240
38	C3P	-3272.5	-240
39	C3P	-3217.5	-240
40	C3P	-3162.5	-240
41	C3P	-3107.5	-240
42	C3N	-3052.5	-240
43	C3N	-2997.5	-240
44	C3N	-2942.5	-240
45	C3N	-2887.5	-240
46	VDD3	-2832.5	-240
47	VDD3	-2777.5	-240
48	VDD3	-2722.5	-240
49	VDD3	-2667.5	-240
50	C2P	-2612.5	-240
51	C2P	-2557.5	-240
52	C2P	-2502.5	-240
53	C2P	-2447.5	-240
54	C2N	-2392.5	-240
55	C2N	-2337.5	-240
56	C2N	-2282.5	-240
57	C2N	-2227.5	-240
58	VDDA	-2172.5	-240
59	VDDA	-2117.5	-240
60	VDDA	-2062.5	-240
61	VDDA	-2007.5	-240
62	VDDA	-1952.5	-240
63	VDDA	-1897.5	-240
64	C1P	-1842.5	-240
65	C1P	-1787.5	-240
66	C1P	-1732.5	-240
67	C1P	-1677.5	-240
68	C1N	-1622.5	-240
69	C1N	-1567.5	-240
70	C1N	-1512.5	-240
71	C1N	-1457.5	-240
72	GND	-1402.5	-240
73	GND	-1347.5	-240
74	GND	-1292.5	-240
75	GND	-1237.5	-240
76	GND	-1182.5	-240
77	VDD	-1127.5	-240
78	VDD	-1072.5	-240
79	VDD	-1017.5	-240
80	VDD	-962.5	-240
81	VDD	-907.5	-240
82	DRV	-852.5	-240
83	DRV	-797.5	-240
84	DRV	-742.5	-240
85	FB_P	-687.5	-240
86	FB_P	-632.5	-240
87	FB_P	-577.5	-240
88	FB_P	-522.5	-240
89	FB_N	-467.5	-240
90	FB_N	-412.5	-240
91	FB_N	-357.5	-240
92	FB_N	-302.5	-240
93	FB	-247.5	-240
94	FB	-192.5	-240
95	P_SET1	-137.5	-240
96	DUM_VDD	-82.5	-240
97	P_SET0	-27.5	-240
98	T_IN1	27.5	-240
99	T_IN2	82.5	-240
100	T_IN3	137.5	-240
101	T_IN4	192.5	-240
102	T_IN5	247.5	-240
103	T_IN6	302.5	-240
104	T_IN7	357.5	-240
105	T_IN8	412.5	-240
106	T_IN9	467.5	-240
107	T_OUT1	522.5	-240
108	T_IN10	577.5	-240
109	T_IN11	632.5	-240
110	AGND	687.5	-240
111	AGND	742.5	-240
112	AGND	797.5	-240
113	AGND	852.5	-240
114	AGND	907.5	-240
115	GND	962.5	-240
116	GND	1017.5	-240
117	GND	1072.5	-240
118	GND	1127.5	-240
119	GND	1182.5	-240
120	VDDIO	1237.5	-240
121	VDDIO	1292.5	-240
122	VDDIO	1347.5	-240
123	VDDIO	1402.5	-240
124	VDDIO	1457.5	-240
125	VDDIO	1512.5	-240
126	T_IN12	1567.5	-240
127	T_IN13	1622.5	-240
128	T_IN14	1677.5	-240
129	T_IN15	1732.5	-240
130	T_IN16	1787.5	-240
131	T_IN17	1842.5	-240
132	T_IN18	1897.5	-240
133	T_IN19	1952.5	-240
134	T_IN20	2007.5	-240
135	T_IN21	2062.5	-240
136	T_IN22	2117.5	-240
137	T_OUT2	2172.5	-240
138	T_OUT3	2227.5	-240
139	T_OUT4	2282.5	-240
140	T_OUT5	2337.5	-240
141	T_OUT6	2392.5	-240
142	T_OUT7	2447.5	-240
143	T_OUT8	2502.5	-240
144	T_OUT9	2557.5	-240
145	T_OUT10	2612.5	-240
146	T_OUT11	2667.5	-240
147	T_OUT12	2722.5	-240
148	T_OUT13	2777.5	-240
149	T_OUT14	2832.5	-240
150	T_OUT15	2887.5	-240
151	T_OUT16	2942.5	-240
152	T_OUT17	2997.5	-240
153	T_OUT18	3052.5	-240

Pad No.	Pad Name	X	Y
154	T_OUT19	3107.5	-240
155	T_OUT20	3162.5	-240
156	T_OUT21	3217.5	-240
157	STB	3272.5	-240
158	STB	3327.5	-240
159	DUMMY	3382.5	-240
160	GRB	3437.5	-240
161	GRB	3492.5	-240
162	CSB	3547.5	-240
163	CSB	3602.5	-240
164	SDA	3657.5	-240
165	SDA	3712.5	-240
166	SCL	3767.5	-240
167	SCL	3822.5	-240
168	DUMMY	3877.5	-240
169	HSYNC	3932.5	-240
170	HSYNC	3987.5	-240
171	VSYNC	4042.5	-240
172	VSYNC	4097.5	-240
173	DCLK	4152.5	-240
174	DCLK	4207.5	-240
175	D07	4262.5	-240
176	D07	4317.5	-240
177	D06	4372.5	-240
178	D06	4427.5	-240
179	D05	4482.5	-240
180	D05	4537.5	-240
181	D04	4592.5	-240
182	D04	4647.5	-240
183	D03	4702.5	-240
184	D03	4757.5	-240
185	D02	4812.5	-240
186	D02	4867.5	-240
187	D01	4922.5	-240
188	D01	4977.5	-240
189	D00	5032.5	-240
190	D00	5087.5	-240
191	T_IN23	5142.5	-240
192	COM2	5197.5	-240
193	COM2	5252.5	-240
194	DUMMY	5307.5	-240
195	DUMMY	5446	227
196	DUMMY	5432	97
197	DUMMY	5418	227
198	COM2	5404	97
199	COM2	5390	227
200	COM2	5376	97
201	COM2	5362	227
202	DUMMY	5348	97
203	DUMMY	5334	227
204	G0	5320	97
205	G2	5306	227
206	G4	5292	97

Pad No.	Pad Name	X	Y
207	G6	5278	227
208	G8	5264	97
209	G10	5250	227
210	G12	5236	97
211	G14	5222	227
212	G16	5208	97
213	G18	5194	227
214	G20	5180	97
215	G22	5166	227
216	G24	5152	97
217	G26	5138	227
218	G28	5124	97
219	G30	5110	227
220	G32	5096	97
221	G34	5082	227
222	G36	5068	97
223	G38	5054	227
224	G40	5040	97
225	G42	5026	227
226	G44	5012	97
227	G46	4998	227
228	G48	4984	97
229	G50	4970	227
230	G52	4956	97
231	G54	4942	227
232	G56	4928	97
233	G58	4914	227
234	G60	4900	97
235	G62	4886	227
236	G64	4872	97
237	G66	4858	227
238	G68	4844	97
239	G70	4830	227
240	G72	4816	97
241	G74	4802	227
242	G76	4788	97
243	G78	4774	227
244	G80	4760	97
245	G82	4746	227
246	G84	4732	97
247	G86	4718	227
248	G88	4704	97
249	G90	4690	227
250	G92	4676	97
251	G94	4662	227
252	G96	4648	97
253	G98	4634	227
254	G100	4620	97
255	G102	4606	227
256	G104	4592	97
257	G106	4578	227
258	G108	4564	97
259	G110	4550	227

Pad No.	Pad Name	X	Y
260	G112	4536	97
261	G114	4522	227
262	G116	4508	97
263	G118	4494	227
264	G120	4480	97
265	G122	4466	227
266	G124	4452	97
267	G126	4438	227
268	G128	4424	97
269	G130	4410	227
270	G132	4396	97
271	G134	4382	227
272	G136	4368	97
273	G138	4354	227
274	G140	4340	97
275	G142	4326	227
276	G144	4312	97
277	G146	4298	227
278	G148	4284	97
279	G150	4270	227
280	G152	4256	97
281	G154	4242	227
282	G156	4228	97
283	G158	4214	227
284	G160	4200	97
285	G162	4186	227
286	G164	4172	97
287	G166	4158	227
288	G168	4144	97
289	G170	4130	227
290	G172	4116	97
291	G174	4102	227
292	G176	4088	97
293	G178	4074	227
294	G180	4060	97
295	G182	4046	227
296	G184	4032	97
297	G186	4018	227
298	G188	4004	97
299	G190	3990	227
300	G192	3976	97
301	G194	3962	227
302	G196	3948	97
303	G198	3934	227
304	G200	3920	97
305	G202	3906	227
306	G204	3892	97
307	G206	3878	227
308	G208	3864	97
309	G210	3850	227
310	G212	3836	97
311	G214	3822	227
312	G216	3808	97

Pad No.	Pad Name	X	Y
313	G218	3794	227
314	G220	3780	97
315	G222	3766	227
316	G224	3752	97
317	G226	3738	227
318	G228	3724	97
319	G230	3710	227
320	G232	3696	97
321	G234	3682	227
322	G236	3668	97
323	G238	3654	227
324	G240	3640	97
325	S1	3514	227
326	S2	3500	97
327	S3	3486	227
328	S4	3472	97
329	S5	3458	227
330	S6	3444	97
331	S7	3430	227
332	S8	3416	97
333	S9	3402	227
334	S10	3388	97
335	S11	3374	227
336	S12	3360	97
337	S13	3346	227
338	S14	3332	97
339	S15	3318	227
340	S16	3304	97
341	S17	3290	227
342	S18	3276	97
343	S19	3262	227
344	S20	3248	97
345	S21	3234	227
346	S22	3220	97
347	S23	3206	227
348	S24	3192	97
349	S25	3178	227
350	S26	3164	97
351	S27	3150	227
352	S28	3136	97
353	S29	3122	227
354	S30	3108	97
355	S31	3094	227
356	S32	3080	97
357	S33	3066	227
358	S34	3052	97
359	S35	3038	227
360	S36	3024	97
361	S37	3010	227
362	S38	2996	97
363	S39	2982	227
364	S40	2968	97
365	S41	2954	227
366	S42	2940	97
367	S43	2926	227
368	S44	2912	97
369	S45	2898	227
370	S46	2884	97
371	S47	2870	227
372	S48	2856	97
373	S49	2842	227
374	S50	2828	97
375	S51	2814	227
376	S52	2800	97
377	S53	2786	227
378	S54	2772	97
379	S55	2758	227
380	S56	2744	97
381	S57	2730	227
382	S58	2716	97
383	S59	2702	227
384	S60	2688	97
385	S61	2674	227
386	S62	2660	97
387	S63	2646	227
388	S64	2632	97
389	S65	2618	227
390	S66	2604	97
391	S67	2590	227
392	S68	2576	97
393	S69	2562	227
394	S70	2548	97
395	S71	2534	227
396	S72	2520	97
397	S73	2506	227
398	S74	2492	97
399	S75	2478	227
400	S76	2464	97
401	S77	2450	227
402	S78	2436	97
403	S79	2422	227
404	S80	2408	97
405	S81	2394	227
406	S82	2380	97
407	S83	2366	227
408	S84	2352	97
409	S85	2338	227
410	S86	2324	97
411	S87	2310	227
412	S88	2296	97
413	S89	2282	227
414	S90	2268	97
415	S91	2254	227
416	S92	2240	97
417	S93	2226	227
418	S94	2212	97
419	S95	2198	227
420	S96	2184	97
421	S97	2170	227
422	S98	2156	97
423	S99	2142	227
424	S100	2128	97
425	S101	2114	227
426	S102	2100	97
427	S103	2086	227
428	S104	2072	97
429	S105	2058	227
430	S106	2044	97
431	S107	2030	227
432	S108	2016	97
433	S109	2002	227
434	S110	1988	97
435	S111	1974	227
436	S112	1960	97
437	S113	1946	227
438	S114	1932	97
439	S115	1918	227
440	S116	1904	97
441	S117	1890	227
442	S118	1876	97
443	S119	1862	227
444	S120	1848	97
445	S121	1834	227
446	S122	1820	97
447	S123	1806	227
448	S124	1792	97
449	S125	1778	227
450	S126	1764	97
451	S127	1750	227
452	S128	1736	97
453	S129	1722	227
454	S130	1708	97
455	S131	1694	227
456	S132	1680	97
457	S133	1666	227
458	S134	1652	97
459	S135	1638	227
460	S136	1624	97
461	S137	1610	227
462	S138	1596	97
463	S139	1582	227
464	S140	1568	97
465	S141	1554	227
466	S142	1540	97
467	S143	1526	227
468	S144	1512	97
469	S145	1498	227
470	S146	1484	97
471	S147	1470	227

Pad No.	Pad Name	X	Y
472	S148	1456	97
473	S149	1442	227
474	S150	1428	97
475	S151	1414	227
476	S152	1400	97
477	S153	1386	227
478	S154	1372	97
479	S155	1358	227
480	S156	1344	97
481	S157	1330	227
482	S158	1316	97
483	S159	1302	227
484	S160	1288	97
485	S161	1274	227
486	S162	1260	97
487	S163	1246	227
488	S164	1232	97
489	S165	1218	227
490	S166	1204	97
491	S167	1190	227
492	S168	1176	97
493	S169	1162	227
494	S170	1148	97
495	S171	1134	227
496	S172	1120	97
497	S173	1106	227
498	S174	1092	97
499	S175	1078	227
500	S176	1064	97
501	S177	1050	227
502	S178	1036	97
503	S179	1022	227
504	S180	1008	97
505	S181	994	227
506	S182	980	97
507	S183	966	227
508	S184	952	97
509	S185	938	227
510	S186	924	97
511	S187	910	227
512	S188	896	97
513	S189	882	227
514	S190	868	97
515	S191	854	227
516	S192	840	97
517	S193	826	227
518	S194	812	97
519	S195	798	227
520	S196	784	97
521	S197	770	227
522	S198	756	97
523	S199	742	227
524	S200	728	97

Pad No.	Pad Name	X	Y
525	S201	714	227
526	S202	700	97
527	S203	686	227
528	S204	672	97
529	S205	658	227
530	S206	644	97
531	S207	630	227
532	S208	616	97
533	S209	602	227
534	S210	588	97
535	S211	574	227
536	S212	560	97
537	S213	546	227
538	S214	532	97
539	S215	518	227
540	S216	504	97
541	S217	490	227
542	S218	476	97
543	S219	462	227
544	S220	448	97
545	S221	434	227
546	S222	420	97
547	S223	406	227
548	S224	392	97
549	S225	378	227
550	S226	364	97
551	S227	350	227
552	S228	336	97
553	S229	322	227
554	S230	308	97
555	S231	294	227
556	S232	280	97
557	S233	266	227
558	S234	252	97
559	S235	238	227
560	S236	224	97
561	S237	210	227
562	S238	196	97
563	S239	182	227
564	S240	168	97
565	DUMMY	70	227
566	DUMMY	56	97
567	DUMMY	42	227
568	DUMMY	28	97
569	DUMMY	14	227
570	DUMMY	0	97
571	DUMMY	-14	227
572	DUMMY	-28	97
573	DUMMY	-42	227
574	DUMMY	-56	97
575	DUMMY	-70	227
576	S241	-168	97
577	S242	-182	227

Pad No.	Pad Name	X	Y
578	S243	-196	97
579	S244	-210	227
580	S245	-224	97
581	S246	-238	227
582	S247	-252	97
583	S248	-266	227
584	S249	-280	97
585	S250	-294	227
586	S251	-308	97
587	S252	-322	227
588	S253	-336	97
589	S254	-350	227
590	S255	-364	97
591	S256	-378	227
592	S257	-392	97
593	S258	-406	227
594	S259	-420	97
595	S260	-434	227
596	S261	-448	97
597	S262	-462	227
598	S263	-476	97
599	S264	-490	227
600	S265	-504	97
601	S266	-518	227
602	S267	-532	97
603	S268	-546	227
604	S269	-560	97
605	S270	-574	227
606	S271	-588	97
607	S272	-602	227
608	S273	-616	97
609	S274	-630	227
610	S275	-644	97
611	S276	-658	227
612	S277	-672	97
613	S278	-686	227
614	S279	-700	97
615	S280	-714	227
616	S281	-728	97
617	S282	-742	227
618	S283	-756	97
619	S284	-770	227
620	S285	-784	97
621	S286	-798	227
622	S287	-812	97
623	S288	-826	227
624	S289	-840	97
625	S290	-854	227
626	S291	-868	97
627	S292	-882	227
628	S293	-896	97
629	S294	-910	227
630	S295	-924	97

Pad No.	Pad Name	X	Y
631	S296	-938	227
632	S297	-952	97
633	S298	-966	227
634	S299	-980	97
635	S300	-994	227
636	S301	-1008	97
637	S302	-1022	227
638	S303	-1036	97
639	S304	-1050	227
640	S305	-1064	97
641	S306	-1078	227
642	S307	-1092	97
643	S308	-1106	227
644	S309	-1120	97
645	S310	-1134	227
646	S311	-1148	97
647	S312	-1162	227
648	S313	-1176	97
649	S314	-1190	227
650	S315	-1204	97
651	S316	-1218	227
652	S317	-1232	97
653	S318	-1246	227
654	S319	-1260	97
655	S320	-1274	227
656	S321	-1288	97
657	S322	-1302	227
658	S323	-1316	97
659	S324	-1330	227
660	S325	-1344	97
661	S326	-1358	227
662	S327	-1372	97
663	S328	-1386	227
664	S329	-1400	97
665	S330	-1414	227
666	S331	-1428	97
667	S332	-1442	227
668	S333	-1456	97
669	S334	-1470	227
670	S335	-1484	97
671	S336	-1498	227
672	S337	-1512	97
673	S338	-1526	227
674	S339	-1540	97
675	S340	-1554	227
676	S341	-1568	97
677	S342	-1582	227
678	S343	-1596	97
679	S344	-1610	227
680	S345	-1624	97
681	S346	-1638	227
682	S347	-1652	97
683	S348	-1666	227
684	S349	-1680	97
685	S350	-1694	227
686	S351	-1708	97
687	S352	-1722	227
688	S353	-1736	97
689	S354	-1750	227
690	S355	-1764	97
691	S356	-1778	227
692	S357	-1792	97
693	S358	-1806	227
694	S359	-1820	97
695	S360	-1834	227
696	S361	-1848	97
697	S362	-1862	227
698	S363	-1876	97
699	S364	-1890	227
700	S365	-1904	97
701	S366	-1918	227
702	S367	-1932	97
703	S368	-1946	227
704	S369	-1960	97
705	S370	-1974	227
706	S371	-1988	97
707	S372	-2002	227
708	S373	-2016	97
709	S374	-2030	227
710	S375	-2044	97
711	S376	-2058	227
712	S377	-2072	97
713	S378	-2086	227
714	S379	-2100	97
715	S380	-2114	227
716	S381	-2128	97
717	S382	-2142	227
718	S383	-2156	97
719	S384	-2170	227
720	S385	-2184	97
721	S386	-2198	227
722	S387	-2212	97
723	S388	-2226	227
724	S389	-2240	97
725	S390	-2254	227
726	S391	-2268	97
727	S392	-2282	227
728	S393	-2296	97
729	S394	-2310	227
730	S395	-2324	97
731	S396	-2338	227
732	S397	-2352	97
733	S398	-2366	227
734	S399	-2380	97
735	S400	-2394	227
736	S401	-2408	97
737	S402	-2422	227
738	S403	-2436	97
739	S404	-2450	227
740	S405	-2464	97
741	S406	-2478	227
742	S407	-2492	97
743	S408	-2506	227
744	S409	-2520	97
745	S410	-2534	227
746	S411	-2548	97
747	S412	-2562	227
748	S413	-2576	97
749	S414	-2590	227
750	S415	-2604	97
751	S416	-2618	227
752	S417	-2632	97
753	S418	-2646	227
754	S419	-2660	97
755	S420	-2674	227
756	S421	-2688	97
757	S422	-2702	227
758	S423	-2716	97
759	S424	-2730	227
760	S425	-2744	97
761	S426	-2758	227
762	S427	-2772	97
763	S428	-2786	227
764	S429	-2800	97
765	S430	-2814	227
766	S431	-2828	97
767	S432	-2842	227
768	S433	-2856	97
769	S434	-2870	227
770	S435	-2884	97
771	S436	-2898	227
772	S437	-2912	97
773	S438	-2926	227
774	S439	-2940	97
775	S440	-2954	227
776	S441	-2968	97
777	S442	-2982	227
778	S443	-2996	97
779	S444	-3010	227
780	S445	-3024	97
781	S446	-3038	227
782	S447	-3052	97
783	S448	-3066	227
784	S449	-3080	97
785	S450	-3094	227
786	S451	-3108	97
787	S452	-3122	227
788	S453	-3136	97
789	S454	-3150	227

Pad No.	Pad Name	X	Y
790	S455	-3164	97
791	S456	-3178	227
792	S457	-3192	97
793	S458	-3206	227
794	S459	-3220	97
795	S460	-3234	227
796	S461	-3248	97
797	S462	-3262	227
798	S463	-3276	97
799	S464	-3290	227
800	S465	-3304	97
801	S466	-3318	227
802	S467	-3332	97
803	S468	-3346	227
804	S469	-3360	97
805	S470	-3374	227
806	S471	-3388	97
807	S472	-3402	227
808	S473	-3416	97
809	S474	-3430	227
810	S475	-3444	97
811	S476	-3458	227
812	S477	-3472	97
813	S478	-3486	227
814	S479	-3500	97
815	S480	-3514	227
816	G241	-3640	97
817	G239	-3654	227
818	G237	-3668	97
819	G235	-3682	227
820	G233	-3696	97
821	G231	-3710	227
822	G229	-3724	97
823	G227	-3738	227
824	G225	-3752	97
825	G223	-3766	227
826	G221	-3780	97
827	G219	-3794	227
828	G217	-3808	97
829	G215	-3822	227
830	G213	-3836	97
831	G211	-3850	227
832	G209	-3864	97
833	G207	-3878	227
834	G205	-3892	97
835	G203	-3906	227
836	G201	-3920	97
837	G199	-3934	227
838	G197	-3948	97
839	G195	-3962	227
840	G193	-3976	97
841	G191	-3990	227
842	G189	-4004	97

Pad No.	Pad Name	X	Y
843	G187	-4018	227
844	G185	-4032	97
845	G183	-4046	227
846	G181	-4060	97
847	G179	-4074	227
848	G177	-4088	97
849	G175	-4102	227
850	G173	-4116	97
851	G171	-4130	227
852	G169	-4144	97
853	G167	-4158	227
854	G165	-4172	97
855	G163	-4186	227
856	G161	-4200	97
857	G159	-4214	227
858	G157	-4228	97
859	G155	-4242	227
860	G153	-4256	97
861	G151	-4270	227
862	G149	-4284	97
863	G147	-4298	227
864	G145	-4312	97
865	G143	-4326	227
866	G141	-4340	97
867	G139	-4354	227
868	G137	-4368	97
869	G135	-4382	227
870	G133	-4396	97
871	G131	-4410	227
872	G129	-4424	97
873	G127	-4438	227
874	G125	-4452	97
875	G123	-4466	227
876	G121	-4480	97
877	G119	-4494	227
878	G117	-4508	97
879	G115	-4522	227
880	G113	-4536	97
881	G111	-4550	227
882	G109	-4564	97
883	G107	-4578	227
884	G105	-4592	97
885	G103	-4606	227
886	G101	-4620	97
887	G99	-4634	227
888	G97	-4648	97
889	G95	-4662	227
890	G93	-4676	97
891	G91	-4690	227
892	G89	-4704	97
893	G87	-4718	227
894	G85	-4732	97
895	G83	-4746	227

Pad No.	Pad Name	X	Y
896	G81	-4760	97
897	G79	-4774	227
898	G77	-4788	97
899	G75	-4802	227
900	G73	-4816	97
901	G71	-4830	227
902	G69	-4844	97
903	G67	-4858	227
904	G65	-4872	97
905	G63	-4886	227
906	G61	-4900	97
907	G59	-4914	227
908	G57	-4928	97
909	G55	-4942	227
910	G53	-4956	97
911	G51	-4970	227
912	G49	-4984	97
913	G47	-4998	227
914	G45	-5012	97
915	G43	-5026	227
916	G41	-5040	97
917	G39	-5054	227
918	G37	-5068	97
919	G35	-5082	227
920	G33	-5096	97
921	G31	-5110	227
922	G29	-5124	97
923	G27	-5138	227
924	G25	-5152	97
925	G23	-5166	227
926	G21	-5180	97
927	G19	-5194	227
928	G17	-5208	97
929	G15	-5222	227
930	G13	-5236	97
931	G11	-5250	227
932	G9	-5264	97
933	G7	-5278	227
934	G5	-5292	97
935	G3	-5306	227
936	G1	-5320	97
937	DUMMY	-5334	227
938	DUMMY	-5348	97
939	COM1	-5362	227
940	COM1	-5376	97
941	COM1	-5390	227
942	COM1	-5404	97
943	DUMMY	-5418	227
944	DUMMY	-5432	97
945	DUMMY	-5446	227

11.5. Alignment Mark

--Alignment Mark coordinate

Left (-5465, -205)

Right (5465, -205)

--Alignment Mark size

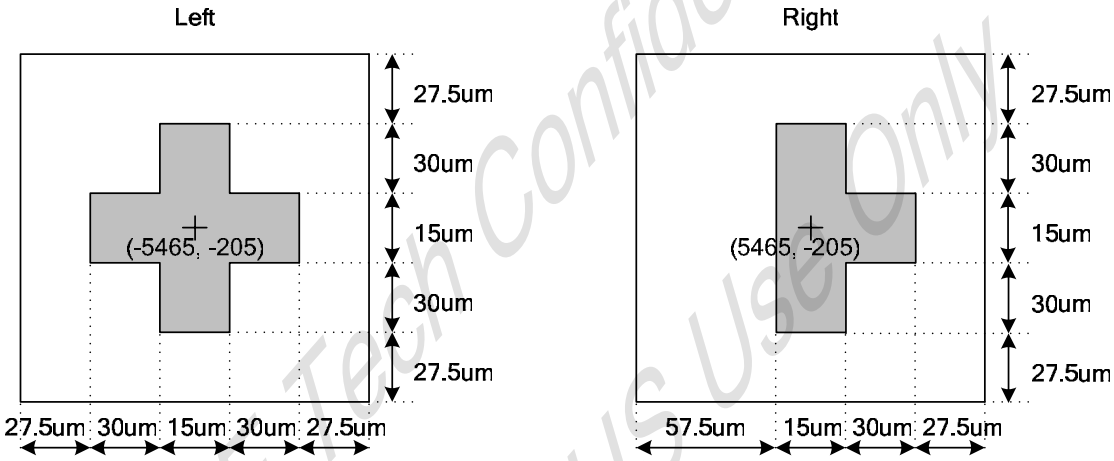


Figure 20: OTA5182A Alignment mark

12. COG PRODUCTS MANUFACTURING GUIDELINES

12.1. Purpose:

The purpose of this specification is to identify ACF bonding process, so that customers can use properly ACF and Chip during the assembly.

12.2. Scope:

ACF bonding process

12.3. Noun definition:

12.3.1. COG: Chip on Glass

12.3.2. ACF (Anisotropic Cunductive Film): .ACF is a functional adhesive tape which is able to connect (conductivity, adhesion, insulation) multiterminals in one time.

12.3.3. CTE: Coefficient of thermal expansion

12.4. Responsibility unity:

ORISETECH Quality Assurance unity

12.5. Contents:

12.5.1. Applicable documents

IPC-SM-782: Surface Mount Design & Land Pattern Standard

IPC-7351Generic Requirements for Surface Mount Design and Land Pattern Standard.

IPC JEDEC: J-STD-033A Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

JESD22-B111: Board Level Drop Test of Components for Handheld Electronic Products

IPC-A-610: Acceptability of Electronic Assemblies

12.5.2. ACF Characteristics:

12.5.2.1. Three factors to achieve the connection: Temperature, Pressure, Time.

12.5.3. ACF process :

12.5.3.1. To use Low Temperature and Low stress ACF is recommended for thin chip as 300 um.

12.5.3.2. Warp issues may happen if customers do not use Low Temperature and Low stress ACF for long chip .And warp issues may induce chip broken after ACF bonding for the CTE mismatch of Glass and ACF and Chip.

12.5.3.3. To use 3um ACF is recommended for BUMP space is less than 13um.

12.5.3.4. To use Low temperature and long time bonding is recommended if delamination happens in edge of chip.

12.5.3.5. For fine pitch and thin chip (300 um) products, customer should review ACF bonding condition with ACF maker.

12.6. References:

*IPC:

http://www.ipc.org

*HDPUG (High Density Package Users Group)

http://www.hdpug.org

*JEDEC (Joint Electronic Device Engineering Council)

http://www.jedec.org

*JEITA (Japan Electronic Industry Association)

http://www.jeita.org

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14. REVISION HISTORY

Date	Revision #	Description	Page
MAR. 10, 2009	0.5	1.Add HDL funcation table 2.Modify Serial communication timing 3.Modified the application notes	12 18.20 31
JAN. 23, 2009	0.4	1. Add relationship between SD input data and output voltages 2. Modify Figure 18 OTA5182A Application example 3. Modify Pad assignment 4. Modify Bump Characteristics. 5. Add Alignment Mark coordinate	14 30 31 32 39
DEC. 01, 2008	0.3	1. Update default setting of S6 and S12 2. Modify PAD Dimension.	8 31
JUL.30, 2008	0.2	Modify Pad name.	5-6 32-39
JUL. 25, 2008	0.1	Original	42