Specification

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Controlled by DCC

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Code Name	100	200	300	400	500	600	700
Dept.	HR	S/M	MFG	R&D	CH	QRA	MIS
	--	✓	✓	✓	✓	✓	--

文件變更履歷頁

Document Change History

版次 Rev.	變更項次 Change Items#	變更內容簡述 Change Description	變更依據文件號碼 ECN #	生效日期 Eff. Date
001	-	New Release		Jun./19/'01
002		P1: Liquid crystal drive voltage: 2.6 to 5.5V->2.6 to 4.5V P4: modify chart for D0~D7 P6: correct charts P9: change application example P10: correct timing chart P12,13:modify V0-GND=2.6 to 5.5-> 2.6 to 4.5V f_{CL1}=19.2MHz->19.2KHz f_M=1.5MHz->1.5KHz P11: correct item 4.2 turned off on-> turned on or off P14: modify notes4 timing chart P15: modify notes1,2 P16:modify CL2 $t_{MH->}t_{HCL}$	E10010007	10/23/2001
003	P15	Clock rise time(MAX20→7ns) Clock fall time(MAX20→7ns)	E01080006	01/24/2008
004				
005				

接續頁 CONTINUATION --- ☐ 是 YES; ■ 否 NO

320-Channel Low-voltage Segment Driver for Dot-Matrix STN Liquid Crystal Display

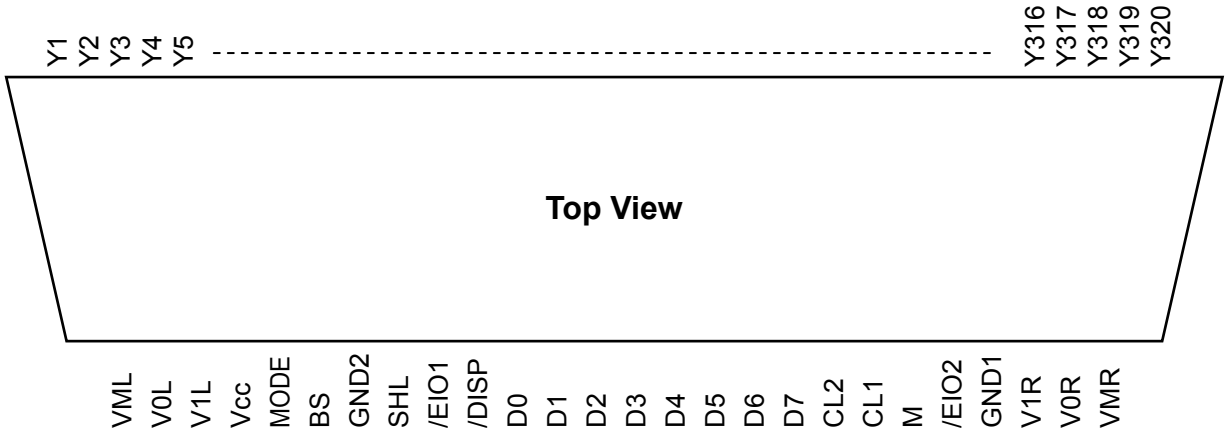
Description

The IST3031 is a 320-channel segment driver for driving a dot-matrix STN liquid-crystal panel at a low voltage. The driver can also correspond to 240-channel output by switching mode. It operates at a low voltage: a liquid-crystal drive voltage of 4.5 V and a logic drive voltage of 3 V, and is used together with common driver IST3032. The package, which adopts a flexible TCP, can be applied to various liquid crystal panels.

Features

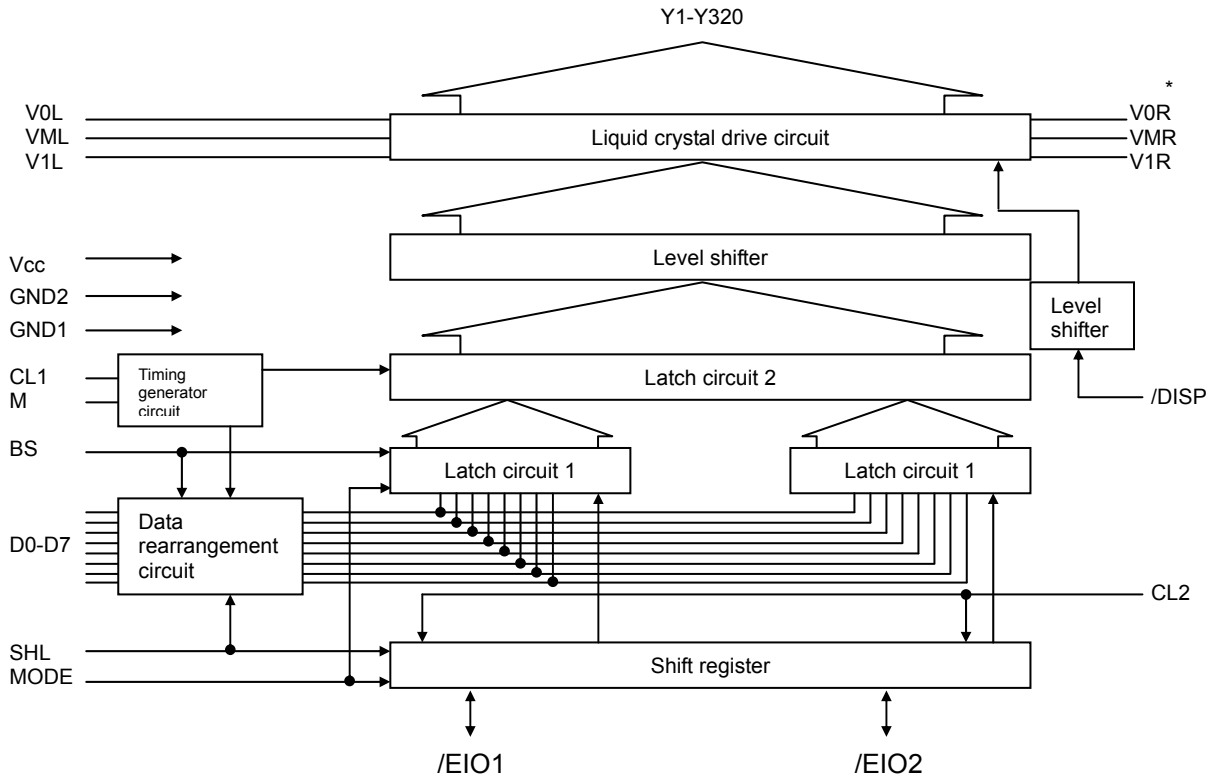
- Display duty: Up to 1/240
- Liquid crystal drive voltage: 2.6 to 4.5 V
- Number of liquid crystal drive circuits: 320 circuits
- Operating voltage: 2.5 to 5.5 V
- Number of data bits: 4 or 8 bits
- Shift clock speed: 8 MHz max/5V
  6.5 MHz max/3V
- Together with the common drivers IST3032
- Low power consumption
- Switching output mode: 320 output mode
  240 output mode
- Display-off function
- Flexible TCP
- Automatic generation of chip-enable signals
- Standby function

Pin Arrangement



Note: TCP dimensions are not defined.

Internal Block Diagram



Note: Pins V0L, VML, and V1L are internally connected to pins V0R, VMR, and V1R, respectively.

1. Liquid crystal drive circuit
   Selects and outputs the liquid crystal drive level V0, VM, or V1 by /DISP and a combination of data for latch circuit 2 and signal M.

2. Level shifter
   Converts logic signals to liquid crystal drive signals.

3. Latch circuit 2
   320-bit latch circuit, which latches the data of latch circuits 1 at the fall of CL1 and outputs the data to the level shifter.

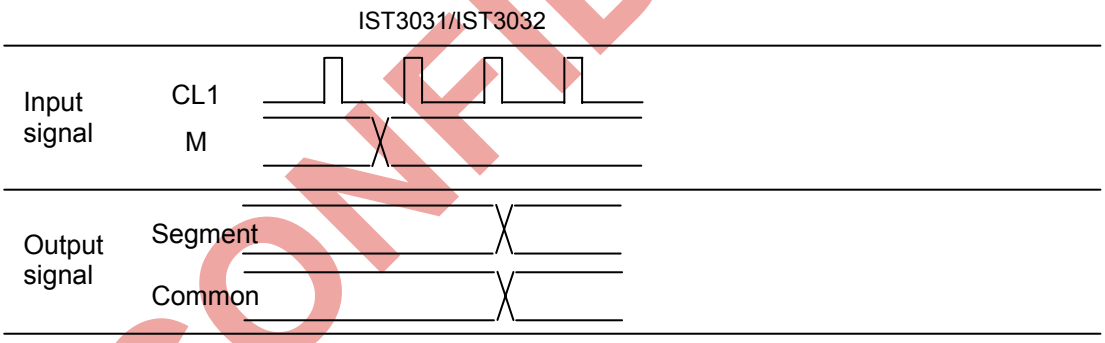
4. Latch circuit 1
   4/8-bit parallel data latch circuit, which latches display data D0 to D7 according to signals transmitted from the shift register.

5. Shift register
   80-bit shift register, which generates data-capture signals for latch circuits 1 at the fall of CL2.

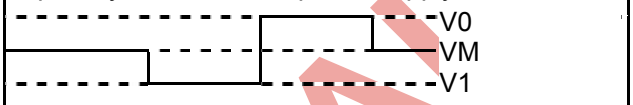
6. Data rearrangement circuit
   Inverts the order of data output crosswise.

7. Timing generator circuit
   The timing generator circuit generates data latch pulses for latch circuit 2 and changes pulse the LCD drive outputs to AC.

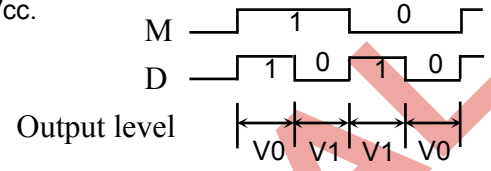
LOW VOLTAGE driver timing



Pin Functions

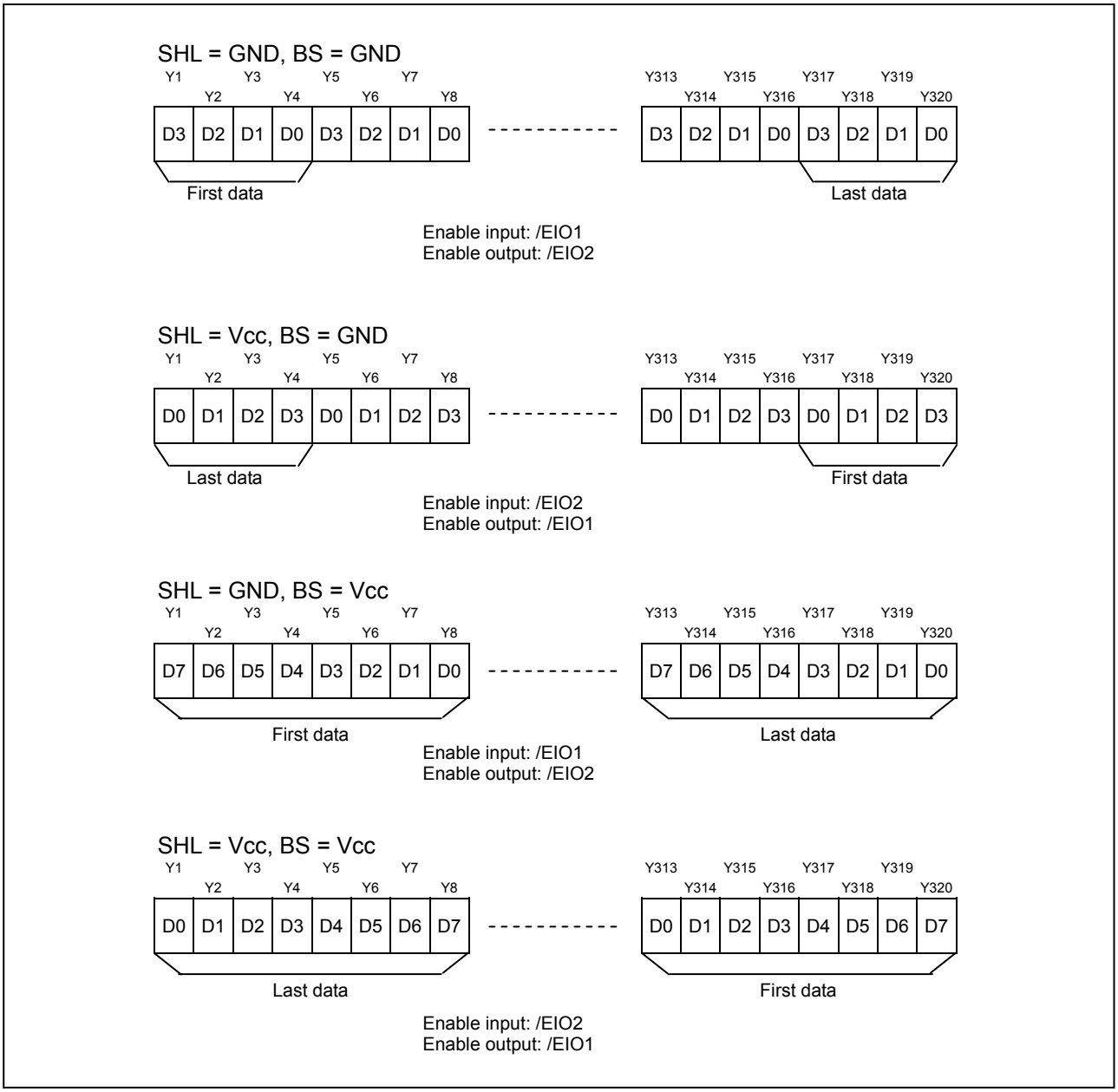
<table>
<tr><th>Class</th><th>Symbol</th><th>Pin Name</th><th>I / O</th><th>Functions</th></tr>
<tr><td rowspan="2">Power supply</td><td>Vcc
GND1
GND2</td><td>Vcc
GND</td><td>-</td><td>Vcc-GND: Power supply for logic.</td></tr>
<tr><td>V0L, R
VML, R
V1L, R</td><td>V0L, R
VML, R
V1L, R</td><td>Input</td><td>Liquid crystal drive level power supply
  </td></tr>
<tr><td rowspan="9">Control signal</td><td>CL1</td><td>Clock 1</td><td>Input</td><td>Latch signal of display data: A liquid crystal drive signal corresponding to display data is output at the fall of CL1.</td></tr>
<tr><td>CL2</td><td>Clock 2</td><td>Input</td><td>Capture signal of display data: Display data is captured at the fall of CL2.</td></tr>
<tr><td>M</td><td>M</td><td>Input</td><td>A.C. signal of liquid crystal drive output</td></tr>
<tr><td>D0 to D7</td><td>DATA 0
to
DATA 7</td><td>Input</td><td>
<table>
<tr><th>Display data t</th><th>liquid crystal drive output</th><th>Liquid crystal display</th></tr>
<tr><td>1</td><td>(Vcc level) Selected level</td><td>ON</td></tr>
<tr><td>0</td><td>(GND level) Not-selected level</td><td>OFF</td></tr>
</table>
</td></tr>
<tr><td>SHL</td><td>Shift Left</td><td>Input</td><td>Control signal for inverting the order of data output (see the page 6)</td></tr>
<tr><td>/EIO1</td><td>Enable IO1</td><td>I / O</td><td>
<table>
<tr><th>SHL</th><th>/EIO1</th><th>/EIO2</th></tr>
<tr><td>GND</td><td>Enable input</td><td>Enable output</td></tr>
<tr><td>Vcc</td><td>Enable output</td><td>Enable input</td></tr>
</table>
</td></tr>
<tr><td>/EIO2</td><td>Enable IO2</td><td>I / O</td><td>Enable input: The enable input of the first IC is connected to the GND and another is connected to the enable input of the second IC.
Enable output: Connected to the enable input of the second IC at cascade output.</td></tr>
<tr><td>/DISP</td><td>Display off</td><td>Input</td><td>Grounding /DISP sets liquid crystal drive output Y1-Y320 to the VM level.</td></tr>
<tr><td>BS</td><td>Bus select</td><td>Input</td><td>Switches the number of input bits for the display data.
Vcc 8-bit input mode
GND 4-bit input mode (Captures data from D0-D3. At this time, connect D4-D7 to the GND.)</td></tr>
<tr><td>MODE</td><td>MODE</td><td>Input</td><td>Switches the number of input bits for the display data.
Vcc 320 output mode
GND 240 output mode (Y41-Y280 are valid output. The other 80 pins output the not-selected level signals synchronized every time, release these pins.)</td></tr>
</table>

Pin Functions (cont)

Class	Symbol	Pin Name	I / O	Functions
Liquid crystal drive output	Y1 to Y320	Y1 to Y320	Output	Liquid crystal drive output: Selects and outputs level V0 or V1 according to the combination of the M signal and display data when /DISP is connected to Vcc. 

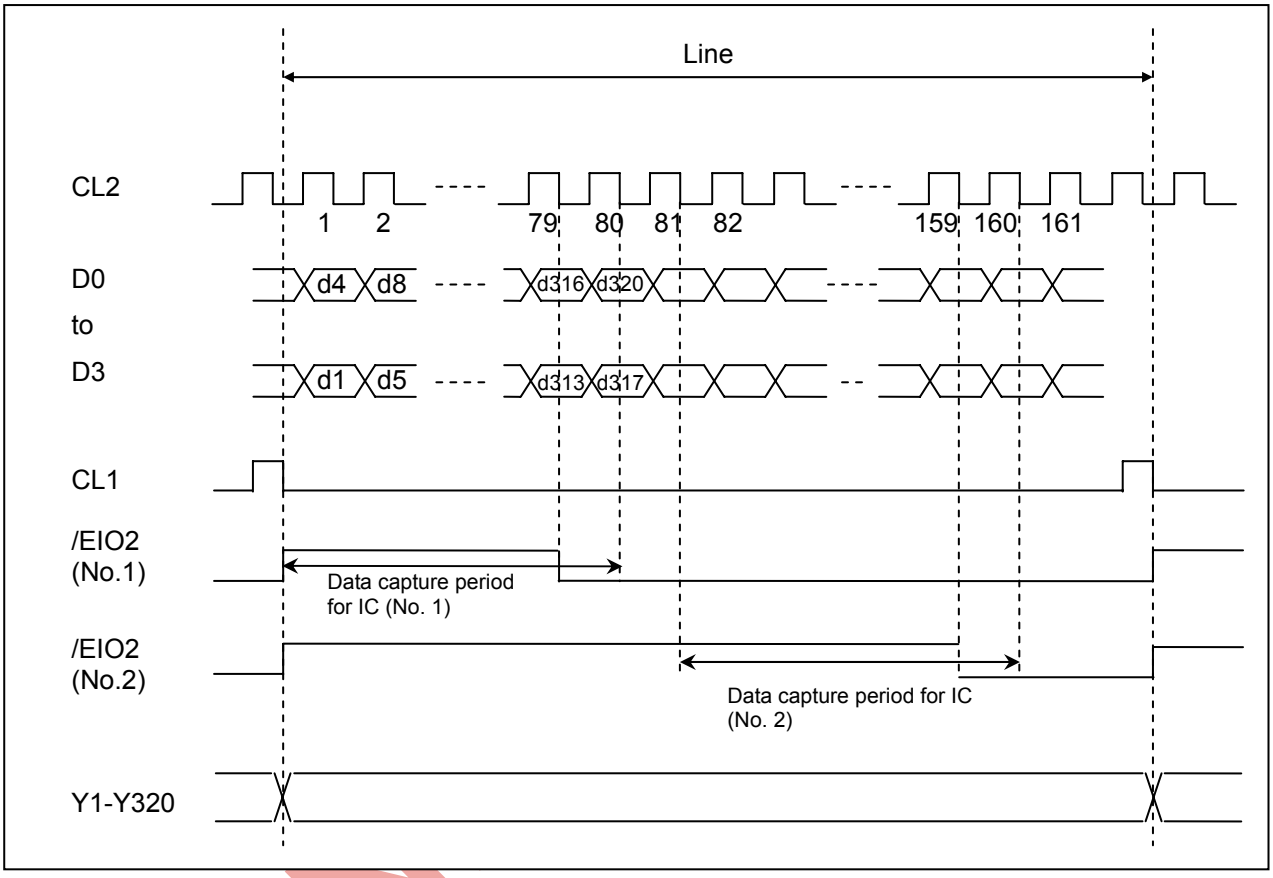
Rearranging Output Data (SHL)

The order for the output of captured data is inverted crosswise according to the SHL signal. At this time, the input/output pin of the enable signal can be switched.



Operation Timing

(1) 4-bit capture mode (1 line, 640 dots)



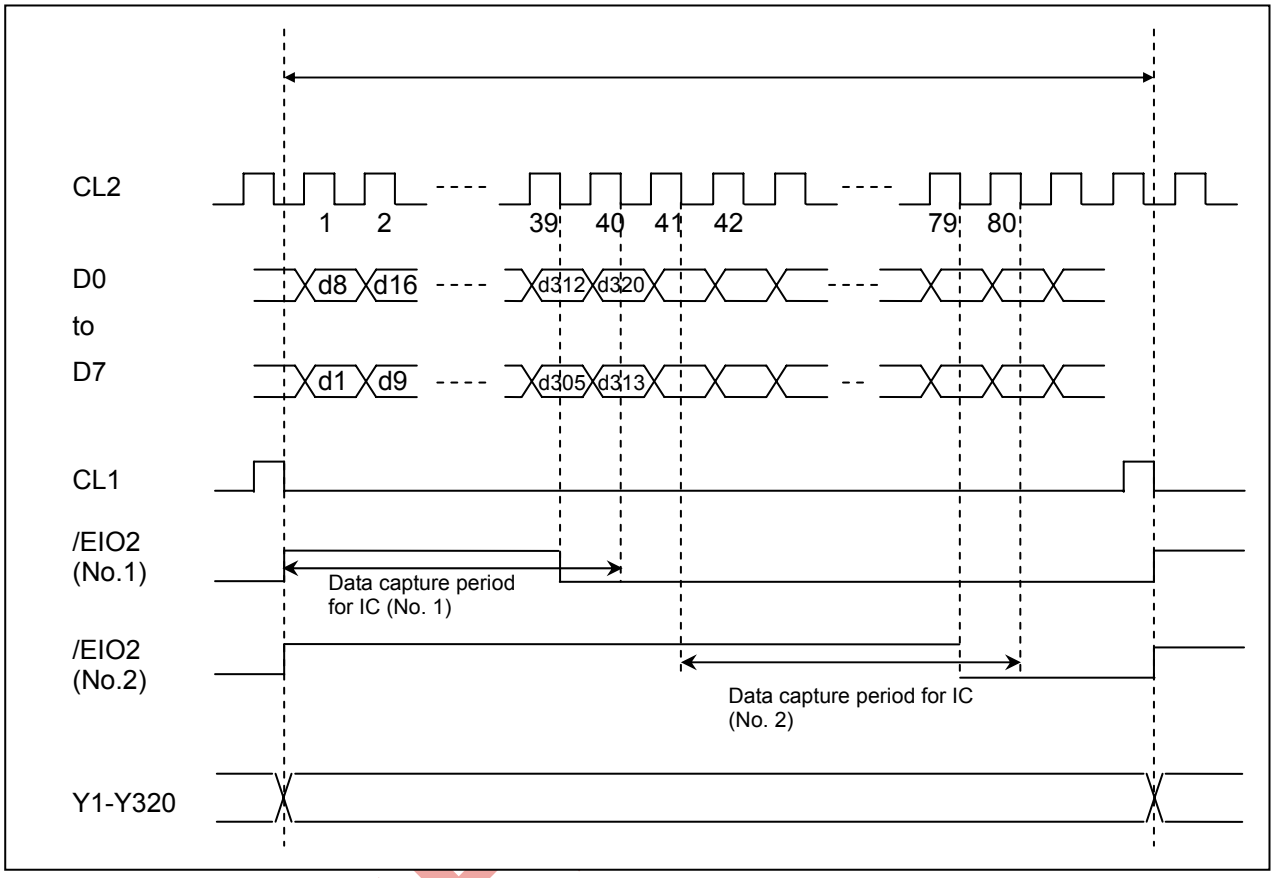
BS = GND (4-bit capture mode)

During the data standby state when the data capture operation enable signal is low (SHL = GND: /EIO1), the next data capture clock (CL2) cancels the standby state. The 4-bit data is captured at the fall of CL2. when 316 bits are captured, the enable signal becomes the GND level (SHL = GND: /EIO2). When 320 bits are captured, the operation automatically stops (the standby state is entered). The second IC is then activated when pin /EIO2 is connected to pin /EIO1 of the second IC.

Data output changes at the fall of CL1.

During SHL = GND, captured data d1 and d320 are output to Y1 and Y320, respectively. During SHL = Vcc, data d1 and d320 are output to Y320 and Y1, respectively.

(2) 8-bit capture mode (1 line, 640 dots)



BS = Vcc (8-bit capture mode)

The 8-bit display data is captured at the fall of CL2. Other basic operations are the same as those of the 4-bit capture mode.

Application Example

Application Example

Figure 1 shows an application example of 320 x 3(color) x 240 dot Quarter VGA Size STN color panel. This panel consist on IST3032 x 1 piece and IST3031 x 3 pieces.
IST3032 generate M signal and DOC signal. M signal pin is connected M signal pin of IST3031 and DOC signal pin is connected DISP signal pin of IST3031
IST3032 is able to generates minus voltage by external capacitor, CO.
VEO pin is connected VEE pin VL pin.

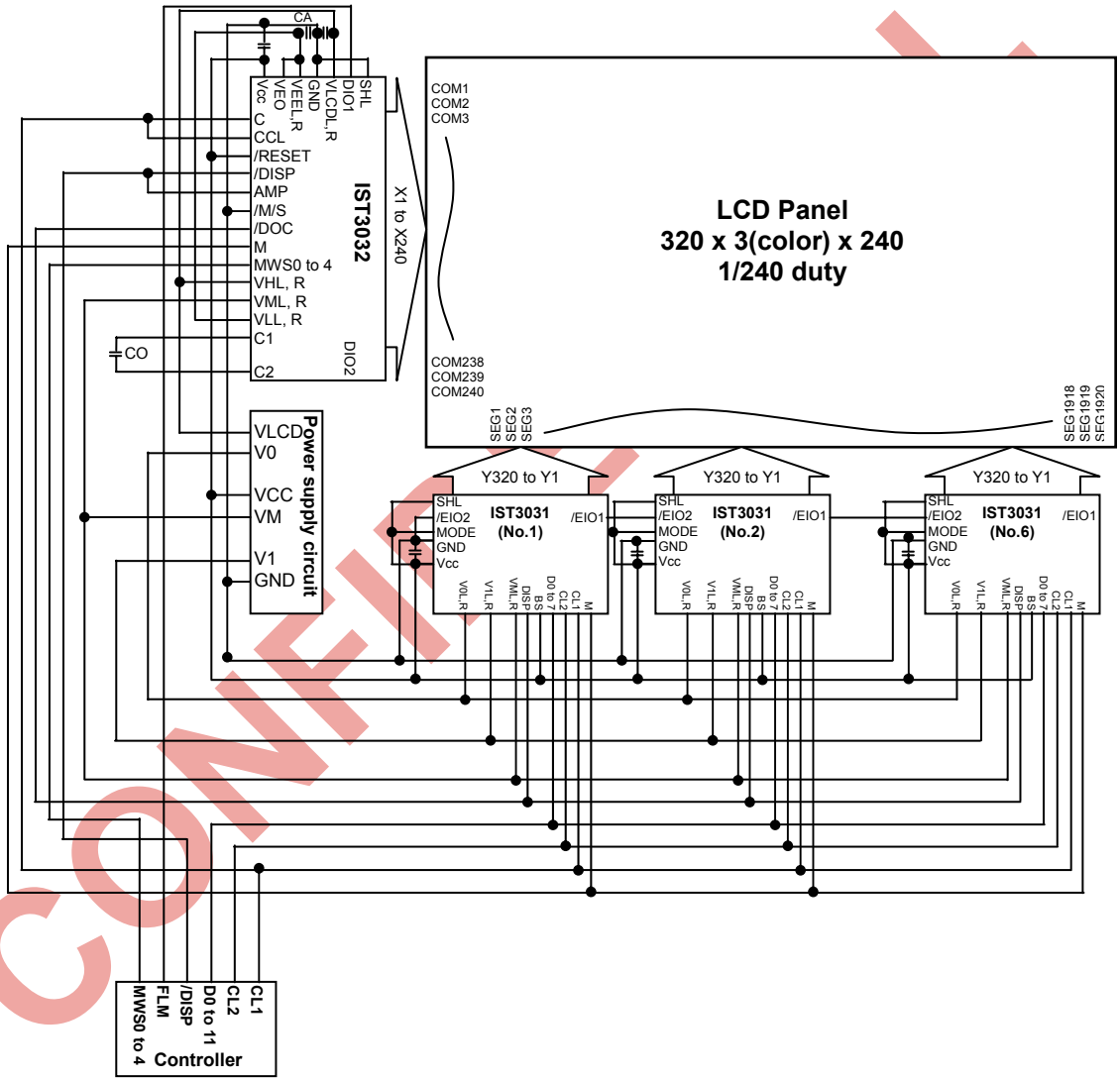


Figure 1 Application Example

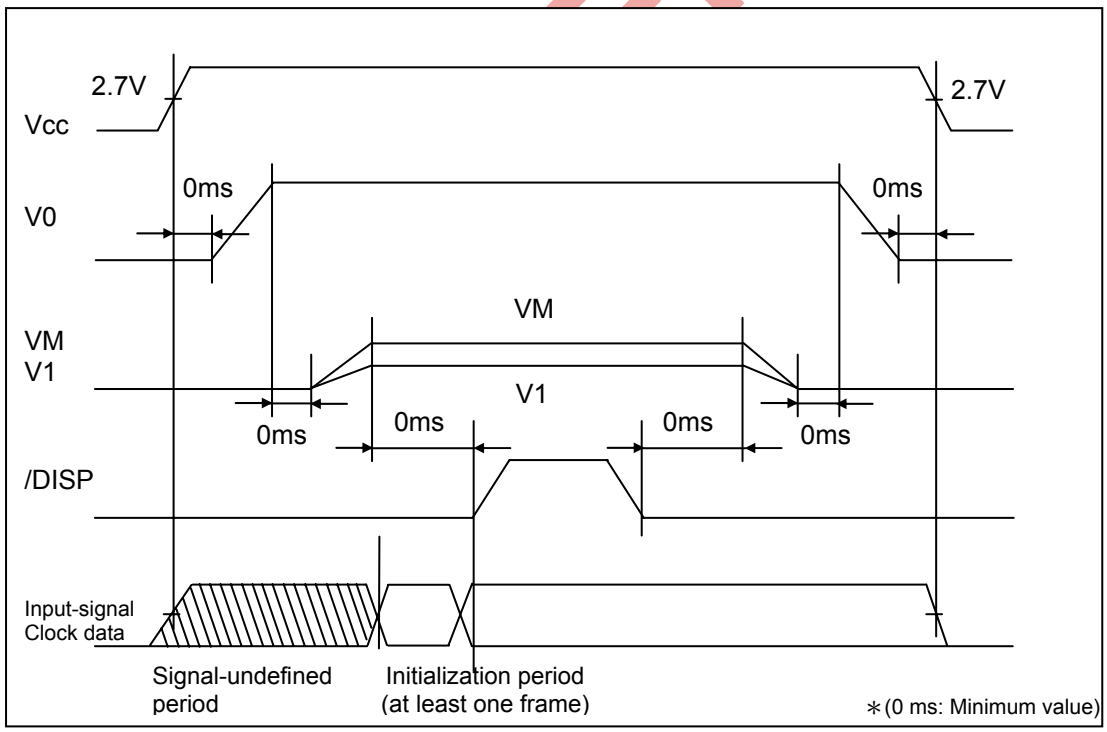
Note:

1. When designing the board, connect a capacitor near the IC to stabilize power supply. Use two capacitors of about 0.1 µF for each IC, between Vcc and GND, V0 and GND, VLCD and GND, and VEE and GND.
2. In addition, for the power supply circuit, connect a capacitor of several µF or several tens of µF between the drive power supply and level power supply in the period between when the liquid-crystal drive power supply is turned on and when it is turned off.
3. when using external capacitor, CO to generate VEE, connect a capacitor of several µF or several tens of µF between the VEE and GND.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Notes
Power supply voltage for logic circuits	V_{CC}	-0.3 to +7.0	V	1,4
Power supply voltage for LCD drive circuits	V0	-0.3 to +7.0	V	1,4
Input voltage 1	VT1	-0.3 to V_{cc} +0.3	V	1,2
Input voltage 2	VT2	-0.3 to V0 +0.3	V	1,3,4
Operating temperature	T_{opr}	-30 to +75	℃	
Storage temperature	T_{stg}	-55 to +110	℃	

Notes: 1. Potential from the GND
2. Applied to pins SHL, /EIO1, /EIO2, /DISP, D0 to D7, CL1, CL2, M, BS, and MODE.
3. Applied to VML, VMR, V1L, and VMR.
Operating the LSI in excess of the absolute maximum rating will result in permanent damage. Use the LSI observing electrical characteristic conditions in normal operation. Exceeding the conditions will cause malfunctions or will affect LSI reliability.
4. Conform to the following turn-on/off sequence of the power and signals. Otherwise, the LSI will malfunction or will be permanently damaged. In addition, LSI reliability will be affected.



4.1 Turning on the power

1) Turn on the power in the order of GND- V_{CC}, GND-V0, and VM/V1. Then, ground the /DISP pin.
2) The LCD forcibly outputs the VM level by the DISPOFF function.
3) Even if an input signal is disturbed immediately after V_{CC} is applied, the DISPOFF function has priority.
4) Input the specific signal to initialize registers in the driver. The initialization period must be at least one frame.
5) The preparation of normal display is completed. Input the V_{CC} level to the /DISP pin to cancel the DISPOFF function. At this time, the level of pins V0, VM, and V1 must rise to the specific potential.

4.2 Turning off the power

The procedure is basically the reverse for turning on the power.

1) Ground the /DISP pin.
2) Turn off the liquid crystal power in the order of VM/V1 and GND-V0.
3) Ground V_{CC} and an input signal.

At this time, the level of pins V0, VM, and V1 must fall to 0 V. Since the DISPOFF function stops when V_{CC} falls to 0 V, the LCD may output a level other than VM. Therefore, a display failure may occur when the power is turned off or on.

Electrical Characteristics

DC Characteristics 1 (V_{CC} = 2.5 to 4.5V, V0-GND = 2.6 to 4.5V, Ta = -30 to +75℃)

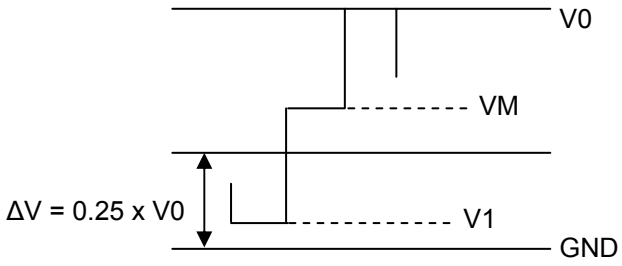
Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	VIH	CL1, CL2, SHL, M, /EIO1, /EIO2, MODE, /DISP, D0 to D7, BS	0.8xV_{CC}	-	V_{CC}	V		
Input low voltage	VIL		0	-	0.2xV_{CC}	V		
Output high voltage	VOH	/EIO1, /EIO2	V_{CC} –0.4	-	-	V	I_{OH}=-0.4mA	
Output low voltage	VOL	/EIO1, /EIO2	-	-	0.4	V	I_{OL}=0.4mA	
Vi-Yj on resistance	R_{ON}	Y1 to Y320, V0L, R	-	0.7	2.0	KΩ	I_{ON}=150μA	1
		Y1 to Y320, VML, R	-	2.0	3.0	KΩ		
		Y1 to Y320, V1L, R	-	0.7	2.0	KΩ		
Input leakage current 1	I_{IL1}	CL1, CL2, SHL, M, /EIO1, /EIO2, MODE, /DISP, D0 to D7, BS	-5.0		5.0	μA	VIN=V_{CC} to GND	
Input leakage current 2	I_{IL2}	VML,R, V1L, R	-25		25	μA	VIN=V0 to GND	
Current consumption 1	I_{CC}	V_{CC}	-	150	300	μA	V_{CC}=3.3V V0=2.7V f_{CL2}=3.5MHz f_{CL1}=19.2KHz f_M=1.5KHz	2
Current consumption 2	IV0	V0L, R	-	60	200	μA		
Current consumption 3	I_{ST}	V_{CC}	-	50	100	μA		2,3

DC Characteristics 2 (V_{CC} = 4.5 to 5.5V, V0-GND = 2.6 to 4.5V, Ta = -30 to +75℃)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	VIH	CL1, CL2, SHL, M, /EIO1, /EIO2, MODE, /DISP, D0 to D7, BS	0.8xV_{CC}	-	V_{CC}	V		
Input low voltage	VIL		0	-	0.2xV_{CC}	V		
Output high voltage	VOH	/EIO1, /EIO2	V_{CC} –0.4	-	-	V	I_{OH}=-0.4mA	
Output low voltage	VOL	/EIO1, /EIO2	-	-	0.4	V	I_{OL}=0.4mA	
Vi-Yj on resistance	R_{ON}	Y1 to Y320, V0L, R	-	0.7	2.0	KΩ	I_{ON}=150μA	1
		Y1 to Y320, VML, R	-	2.0	3.0	KΩ		
		Y1 to Y320, V1L, R	-	0.7	2.0	KΩ		
Input leakage current 1	I_{IL1}	CL1, CL2, SHL, M, /EIO1, /EIO2, MODE, /DISP, D0 to D7, BS	-5.0		5.0	μA	VIN=V_{CC} to GND	
Input leakage current 2	I_{IL2}	VML, R, V1L, R	-25		25	μA	VIN=V0 to GND	
Current consumption 1	I_{CC}	V_{CC}	-	230	450	μA	V_{CC}=5.0V V0=2.7V f_{CL2}=3.5MHz f_{CL1}=19.2KHz f_M=1.5KHz	2
Current consumption 2	IV0	V0L, R	-	60	200	μA		
Current consumption 3	I_{ST}	V_{CC}	-	80	150	μA		2,3

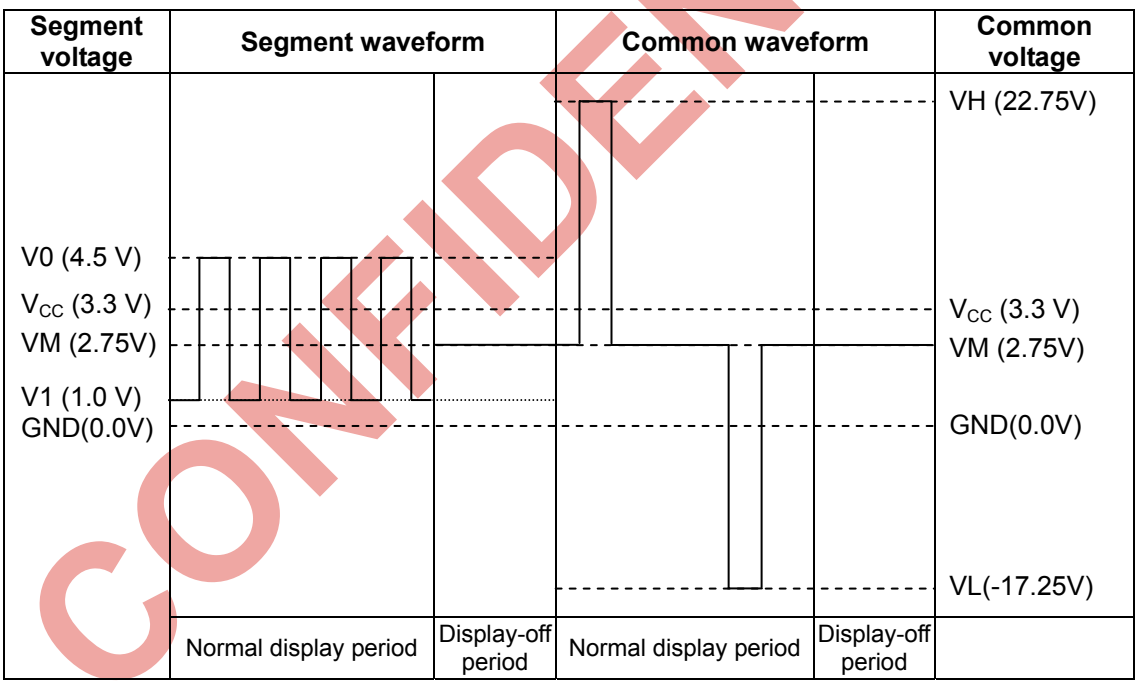
Notes: 1. Resistance between pins Y and V when a load current flows to one of the pins from Y1 to Y320.
The following conditions are defined:
V0-GND = 4.5 V
VM = (V0 + V1)/2
V1 = GND + 1.0

The voltage range of the liquid crystal drive level power supply is described. A voltage around the GND is applied to pin V1, and an intermediate voltage of about V0 and V1 is applied to pin VM. Use the V1 in the range of ΔV = 0.25 x V0, in which the impedance Ron of driver output is stable.



Relationship between the driver output waveform and each level voltage

2. A current flowing in the input or output section is excluded. If an input signal is at an intermediate level for the CMOS, a through-current flows in the input circuit and power supply current increases. Therefore, VIH must be at the V_{CC} level and VIL must be at the GND level.
3. Current at standby
4. The voltage of each signal is shown below.



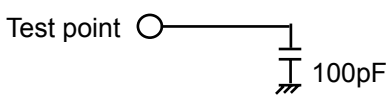
AC Characteristics 1 (V_{CC} = 2.5 to 4.5V, V0-GND = 2.6 to 4.5V, Ta = -30 to +75℃)

Item	Symbol	Pins	Min	Max	Unit
Clock cycle time	t_{CYC}	CL2	152	-	ns
Clock high pulse width 1	t_{CWH2}	CL2	65	-	ns
Clock low pulse width 1	t_{CWL2}	CL2	65	-	ns
Clock high pulse width 2	t_{CWH1}	CL1	65	-	ns
Clock setup time	t_{SCL}	CL1, CL2	80	-	ns
Clock hold time	t_{HCL}	CL1, CL2	80	-	ns
Clock rise time	t_r	CL1, CL2	-	30	ns
Clock fall time	t_f	CL1, CL2	-	30	ns
Data setup time	t_{DS}	D0 to D7, CL2	50	-	ns
Data hold time	t_{DH}	D0 to D7, CL2	50	-	ns
M setup time	t_{MS}	M, CL1	20	-	ns
M hold time	t_{MH}	M, CL1	20	-	ns
Output delay time	t_{pd1}	CL1, Y1 to Y320	-	1000	ns

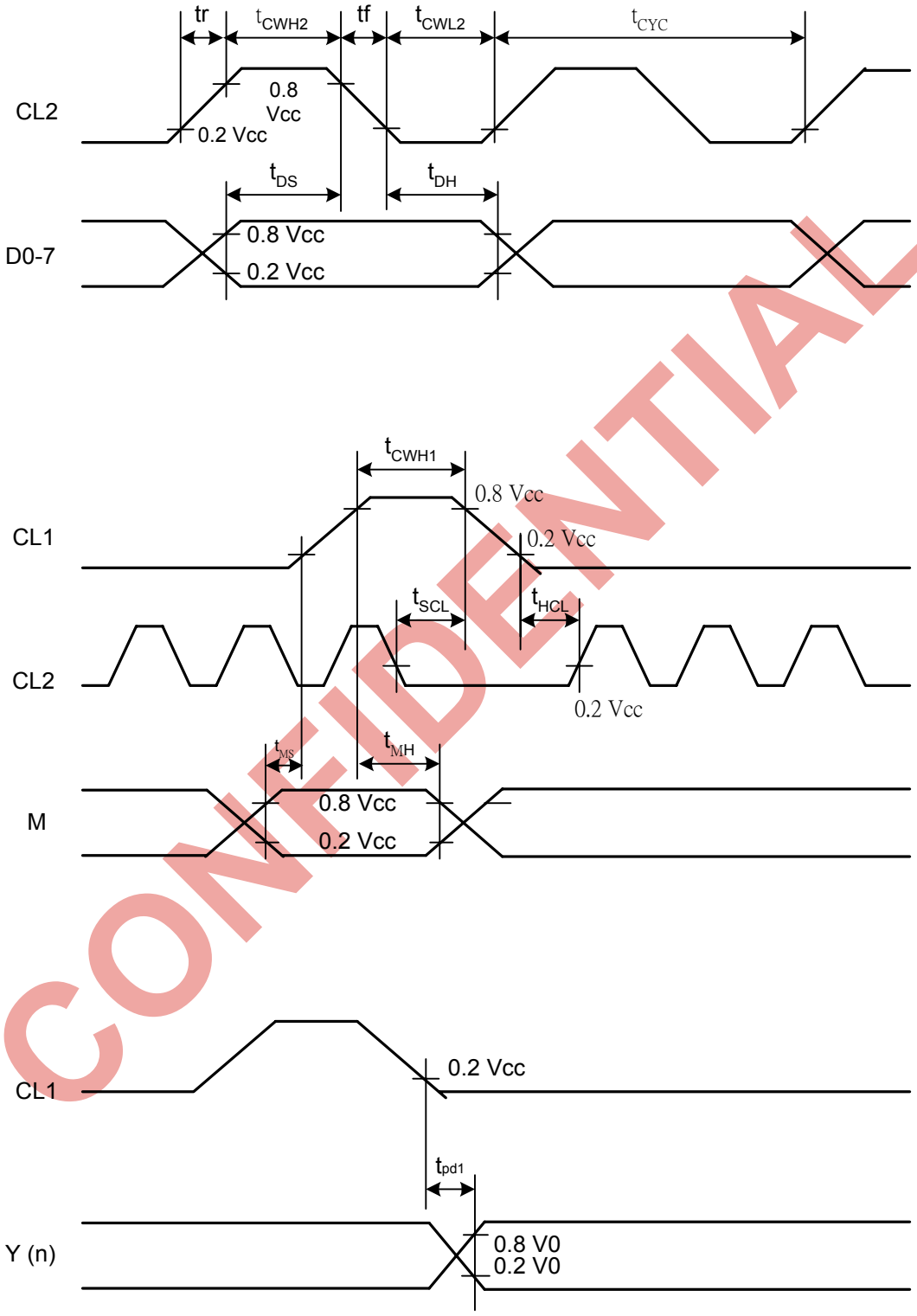
AC Characteristics 2 (V_{CC} = 4.5 to 5.5V, V0-GND = 2.6 to 4.5V, Ta = -30 to +75℃)

Item	Symbol	Pins	Min	Max	Unit
Clock cycle time	t_{CYC}	CL2	125	-	ns
Clock high pulse width 1	t_{CWH2}	CL2	45	-	ns
Clock low pulse width 1	t_{CWL2}	CL2	45	-	ns
Clock high pulse width 2	t_{CWH1}	CL1	45	-	ns
Clock setup time	t_{SCL}	CL1, CL2	80	-	ns
Clock hold time	t_{HCL}	CL1, CL2	80	-	ns
Clock rise time	t_r	CL1, CL2	-	7	ns
Clock fall time	t_f	CL1, CL2	-	7	ns
Data setup time	t_{DS}	D0 to D7, CL2	20	-	ns
Data hold time	t_{DH}	D0 to D7, CL2	20	-	ns
M setup time	t_{MS}	M, CL1	20	-	ns
M hold time	t_{MH}	M, CL1	20	-	ns
Output delay time	t_{pd1}	CL1, Y1 to Y320	-	1000	ns

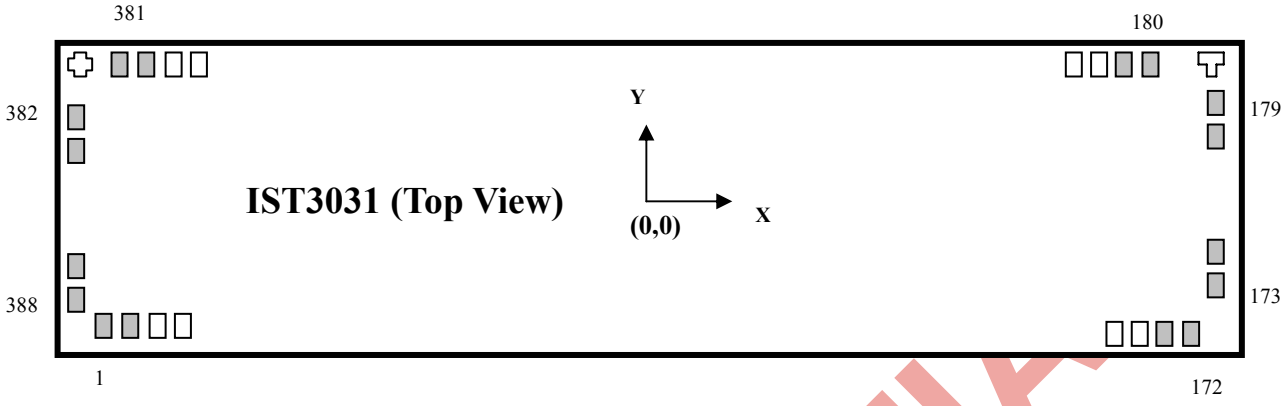
Notes: 1. A load must be 10pF or less for EI/O connection between drivers.
2. For output delay time, connect the load circuit shown below.



IST3031

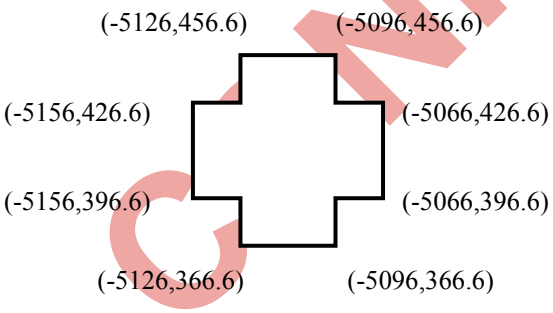


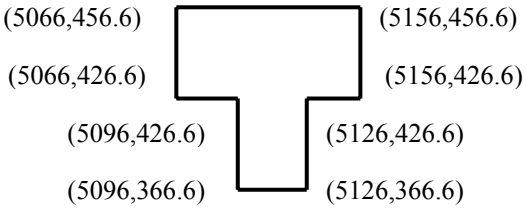
IST3031 PAD CONFIGURATION



	Pad No.	X (um)	Y (um)
Chip Size	388 (total)	10480	1080
Bump size	1 ~ 388	38	80

Pad No	Min pad pitch (um)	Min pad space (um)
1~172	55	17
173~179 382~388	92	12
180~381	50	12





IST3031 PAD CENTER COORDINATES

Pad No	Pad Name	X	Y	Pad No	Pad Name	X	Y	Pad No	Pad Name	X	Y
1	DUMMY	-5055	-416	51	Y13	-2305	-416	101	V1	1015	-416
2	DUMMY	-5000	-416	52	Y12	-2250	-416	102	V1	1085	-416
3	Y61	-4945	-416	53	Y11	-2195	-416	103	V1	1155	-416
4	Y60	-4890	-416	54	Y10	-2140	-416	104	V0	1225	-416
5	Y59	-4835	-416	55	Y9	-2085	-416	105	V0	1295	-416
6	Y58	-4780	-416	56	Y8	-2030	-416	106	V0	1365	-416
7	Y57	-4725	-416	57	Y7	-1975	-416	107	VM	1435	-416
8	Y56	-4670	-416	58	Y6	-1920	-416	108	VM	1505	-416
9	Y55	-4615	-416	59	Y5	-1865	-416	109	VM	1575	-416
10	Y54	-4560	-416	60	Y4	-1810	-416	110	Y320	1645	-416
11	Y53	-4505	-416	61	Y3	-1755	-416	111	Y319	1700	-416
12	Y52	-4450	-416	62	Y2	-1700	-416	112	Y318	1755	-416
13	Y51	-4395	-416	63	Y1	-1645	-416	113	Y317	1810	-416
14	Y50	-4340	-416	64	VM	-1575	-416	114	Y316	1865	-416
15	Y49	-4285	-416	65	VM	-1505	-416	115	Y315	1920	-416
16	Y48	-4230	-416	66	VM	-1435	-416	116	Y314	1975	-416
17	Y47	-4175	-416	67	V0	-1365	-416	117	Y313	2030	-416
18	Y46	-4120	-416	68	V0	-1295	-416	118	Y312	2085	-416
19	Y45	-4065	-416	69	V0	-1225	-416	119	Y311	2140	-416
20	Y44	-4010	-416	70	V1	-1155	-416	120	Y310	2195	-416
21	Y43	-3955	-416	71	V1	-1085	-416	121	Y309	2250	-416
22	Y42	-3900	-416	72	V1	-1015	-416	122	Y308	2305	-416
23	Y41	-3845	-416	73	VDD	-945	-416	123	Y307	2360	-416
24	Y40	-3790	-416	74	VDD	-875	-416	124	Y306	2415	-416
25	Y39	-3735	-416	75	VDD	-805	-416	125	Y305	2470	-416
26	Y38	-3680	-416	76	MODE	-735	-416	126	Y304	2525	-416
27	Y37	-3625	-416	77	GND	-665	-416	127	Y303	2580	-416
28	Y36	-3570	-416	78	VDD	-595	-416	128	Y302	2635	-416
29	Y35	-3515	-416	79	BS	-525	-416	129	Y301	2690	-416
30	Y34	-3460	-416	80	GND	-455	-416	130	Y300	2745	-416
31	Y33	-3405	-416	81	GND	-385	-416	131	Y299	2800	-416
32	Y32	-3350	-416	82	SHL	-315	-416	132	Y298	2855	-416
33	Y31	-3295	-416	83	VDD	-245	-416	133	Y297	2910	-416
34	Y30	-3240	-416	84	EIO1	-175	-416	134	Y296	2965	-416
35	Y29	-3185	-416	85	NDISPOFF	-105	-416	135	Y295	3020	-416
36	Y28	-3130	-416	86	DI0	-35	-416	136	Y294	3075	-416
37	Y27	-3075	-416	87	DI1	35	-416	137	Y293	3130	-416
38	Y26	-3020	-416	88	DI2	105	-416	138	Y292	3185	-416
39	Y25	-2965	-416	89	DI3	175	-416	139	Y291	3240	-416
40	Y24	-2910	-416	90	DI4	245	-416	140	Y290	3295	-416
41	Y23	-2855	-416	91	DI5	315	-416	141	Y289	3350	-416
42	Y22	-2800	-416	92	DI6	385	-416	142	Y288	3405	-416
43	Y21	-2745	-416	93	DI7	455	-416	143	Y287	3460	-416
44	Y20	-2690	-416	94	GND	525	-416	144	Y286	3515	-416
45	Y19	-2635	-416	95	XCK	595	-416	145	Y285	3570	-416
46	Y18	-2580	-416	96	LP	665	-416	146	Y284	3625	-416
47	Y17	-2525	-416	97	M	735	-416	147	Y283	3680	-416
48	Y16	-2470	-416	98	EIO2	805	-416	148	Y282	3735	-416
49	Y15	-2415	-416	99	GND	875	-416	149	Y281	3790	-416
50	Y14	-2360	-416	100	GND	945	-416	150	Y280	3845	-416

Pad No	Pad Name	X	Y	Pad No	Pad Name	X	Y	Pad No	Pad Name	X	Y
151	Y279	3900	-416	201	Y240	3975	414.3	251	Y190	1475	414.3
152	Y278	3955	-416	202	Y239	3925	414.3	252	Y189	1425	414.3
153	Y277	4010	-416	203	Y238	3875	414.3	253	Y188	1375	414.3
154	Y276	4065	-416	204	Y237	3825	414.3	254	Y187	1325	414.3
155	Y275	4120	-416	205	Y236	3775	414.3	255	Y186	1275	414.3
156	Y274	4175	-416	206	Y235	3725	414.3	256	Y185	1225	414.3
157	Y273	4230	-416	207	Y234	3675	414.3	257	Y184	1175	414.3
158	Y272	4285	-416	208	Y233	3625	414.3	258	Y183	1125	414.3
159	Y271	4340	-416	209	Y232	3575	414.3	259	Y182	1075	414.3
160	Y270	4395	-416	210	Y231	3525	414.3	260	Y181	1025	414.3
161	Y269	4450	-416	211	Y230	3475	414.3	261	Y180	975	414.3
162	Y268	4505	-416	212	Y229	3425	414.3	262	Y179	925	414.3
163	Y267	4560	-416	213	Y228	3375	414.3	263	Y178	875	414.3
164	Y266	4615	-416	214	Y227	3325	414.3	264	Y177	825	414.3
165	Y265	4670	-416	215	Y226	3275	414.3	265	Y176	775	414.3
166	Y264	4725	-416	216	Y225	3225	414.3	266	Y175	725	414.3
167	Y263	4780	-416	217	Y224	3175	414.3	267	Y174	675	414.3
168	Y262	4835	-416	218	Y223	3125	414.3	268	Y173	625	414.3
169	Y261	4890	-416	219	Y222	3075	414.3	269	Y172	575	414.3
170	Y260	4945	-416	220	Y221	3025	414.3	270	Y171	525	414.3
171	DUMMY	5000	-416	221	Y220	2975	414.3	271	Y170	475	414.3
172	DUMMY	5055	-416	222	Y219	2925	414.3	272	Y169	425	414.3
173	DUMMY	5134	-268.7	223	Y218	2875	414.3	273	Y168	375	414.3
174	DUMMY	5134	-176.7	224	Y217	2825	414.3	274	Y167	325	414.3
175	DUMMY	5134	-84.7	225	Y216	2775	414.3	275	Y166	275	414.3
176	DUMMY	5134	7.3	226	Y215	2725	414.3	276	Y165	225	414.3
177	DUMMY	5134	99.3	227	Y214	2675	414.3	277	Y164	175	414.3
178	DUMMY	5134	191.3	228	Y213	2625	414.3	278	Y163	125	414.3
179	DUMMY	5134	283.3	229	Y212	2575	414.3	279	Y162	75	414.3
180	DUMMY	5025	414.3	230	Y211	2525	414.3	280	Y161	25	414.3
181	DUMMY	4975	414.3	231	Y210	2475	414.3	281	Y160	-25	414.3
182	Y259	4925	414.3	232	Y209	2425	414.3	282	Y159	-75	414.3
183	Y258	4875	414.3	233	Y208	2375	414.3	283	Y158	-125	414.3
184	Y257	4825	414.3	234	Y207	2325	414.3	284	Y157	-175	414.3
185	Y256	4775	414.3	235	Y206	2275	414.3	285	Y156	-225	414.3
186	Y255	4725	414.3	236	Y205	2225	414.3	286	Y155	-275	414.3
187	Y254	4675	414.3	237	Y204	2175	414.3	287	Y154	-325	414.3
188	Y253	4625	414.3	238	Y203	2125	414.3	288	Y153	-375	414.3
189	Y252	4575	414.3	239	Y202	2075	414.3	289	Y152	-425	414.3
190	Y251	4525	414.3	240	Y201	2025	414.3	290	Y151	-475	414.3
191	Y250	4475	414.3	241	Y200	1975	414.3	291	Y150	-525	414.3
192	Y249	4425	414.3	242	Y199	1925	414.3	292	Y149	-575	414.3
193	Y248	4375	414.3	243	Y198	1875	414.3	293	Y148	-625	414.3
194	Y247	4325	414.3	244	Y197	1825	414.3	294	Y147	-675	414.3
195	Y246	4275	414.3	245	Y196	1775	414.3	295	Y146	-725	414.3
196	Y245	4225	414.3	246	Y195	1725	414.3	296	Y145	-775	414.3
197	Y244	4175	414.3	247	Y194	1675	414.3	297	Y144	-825	414.3
198	Y243	4125	414.3	248	Y193	1625	414.3	298	Y143	-875	414.3
199	Y242	4075	414.3	249	Y192	1575	414.3	299	Y142	-925	414.3
200	Y241	4025	414.3	250	Y191	1525	414.3	300	Y141	-975	414.3

Pad No	Pad Name	X	Y
301	Y140	-1025	414.3
302	Y139	-1075	414.3
303	Y138	-1125	414.3
304	Y137	-1175	414.3
305	Y136	-1225	414.3
306	Y135	-1275	414.3
307	Y134	-1325	414.3
308	Y133	-1375	414.3
309	Y132	-1425	414.3
310	Y131	-1475	414.3
311	Y130	-1525	414.3
312	Y129	-1575	414.3
313	Y128	-1625	414.3
314	Y127	-1675	414.3
315	Y126	-1725	414.3
316	Y125	-1775	414.3
317	Y124	-1825	414.3
318	Y123	-1875	414.3
319	Y122	-1925	414.3
320	Y121	-1975	414.3
321	Y120	-2025	414.3
322	Y119	-2075	414.3
323	Y118	-2125	414.3
324	Y117	-2175	414.3
325	Y116	-2225	414.3
326	Y115	-2275	414.3
327	Y114	-2325	414.3
328	Y113	-2375	414.3
329	Y112	-2425	414.3
330	Y111	-2475	414.3
331	Y110	-2525	414.3
332	Y109	-2575	414.3
333	Y108	-2625	414.3
334	Y107	-2675	414.3
335	Y106	-2725	414.3
336	Y105	-2775	414.3
337	Y104	-2825	414.3
338	Y103	-2875	414.3
339	Y102	-2925	414.3
340	Y101	-2975	414.3
341	Y100	-3025	414.3
342	Y99	-3075	414.3
343	Y98	-3125	414.3
344	Y97	-3175	414.3
345	Y96	-3225	414.3
346	Y95	-3275	414.3
347	Y94	-3325	414.3
348	Y93	-3375	414.3
349	Y92	-3425	414.3
350	Y91	-3475	414.3
351	Y90	-3525	414.3
352	Y89	-3575	414.3
353	Y88	-3625	414.3
354	Y87	-3675	414.3
355	Y86	-3725	414.3
356	Y85	-3775	414.3
357	Y84	-3825	414.3
358	Y83	-3875	414.3
359	Y82	-3925	414.3
360	Y81	-3975	414.3
361	Y80	-4025	414.3
362	Y79	-4075	414.3
363	Y78	-4125	414.3
364	Y77	-4175	414.3
365	Y76	-4225	414.3
366	Y75	-4275	414.3
367	Y74	-4325	414.3
368	Y73	-4375	414.3
369	Y72	-4425	414.3
370	Y71	-4475	414.3
371	Y70	-4525	414.3
372	Y69	-4575	414.3
373	Y68	-4625	414.3
374	Y67	-4675	414.3
375	Y66	-4725	414.3
376	Y65	-4775	414.3
377	Y64	-4825	414.3
378	Y63	-4875	414.3
379	Y62	-4925	414.3
380	DUMMY	-4975	414.3
381	DUMMY	-5025	414.3
382	DUMMY	-5134	283.3
383	DUMMY	-5134	191.3
384	DUMMY	-5134	99.3
385	DUMMY	-5134	7.3
386	DUMMY	-5134	-84.7
387	DUMMY	-5134	-176.7
388	DUMMY	-5134	-268.7