Specification

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Code Name	100	200	300	400	500	600	700
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文件變更履歷頁
Document Change History

版次 Rev.	變更項次 Change Items#	變更內容簡述 Change Description	變更依據文件號碼 ECN #	生效日期 Eff. Date
001	-	New Release	E01030005	1/30/2003
002	Page1~27	配合進入正式量產(3/06/2003)階段,刪除各首頁之 Preliminary 字樣	E03030004	3/07/2003
003	Page 23	Bump pad size change	E20040001	2/06/2004

接續頁 CONTINUATION --- ■ 是 YES; □ 否 NO

IST3025 160-output LCD Segment/Common Driver IC

DESCRIPTION

The IST3025 is a 160-output segment/common driver IC suitable for driving medium size dot matrix LCD panels. The IST3025 is good both segment driver and common driver, and suitable for a low power consuming, high-precision LCD.

FEATURES

- Number of LCD drive outputs:160
- Supply voltage for the logic system:+2.5 to +5.5 V
- Supply voltage for LCD drive:+10.0 to + 40.0 V
- Low power consumption
- Low output impedance
- Operating temperature:-30 to +85℃
- Package：TCP(Tape Carrier Package)/ Gold Bumped Chip

(Segment mode)

- Shift clock frequency：8 MHz(MAX)
- 4-bit/8-bit parallel input modes are selectable with a mode(MD)pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 160 bits of input date
- Line latch circuits are reset when /DISPOFF active

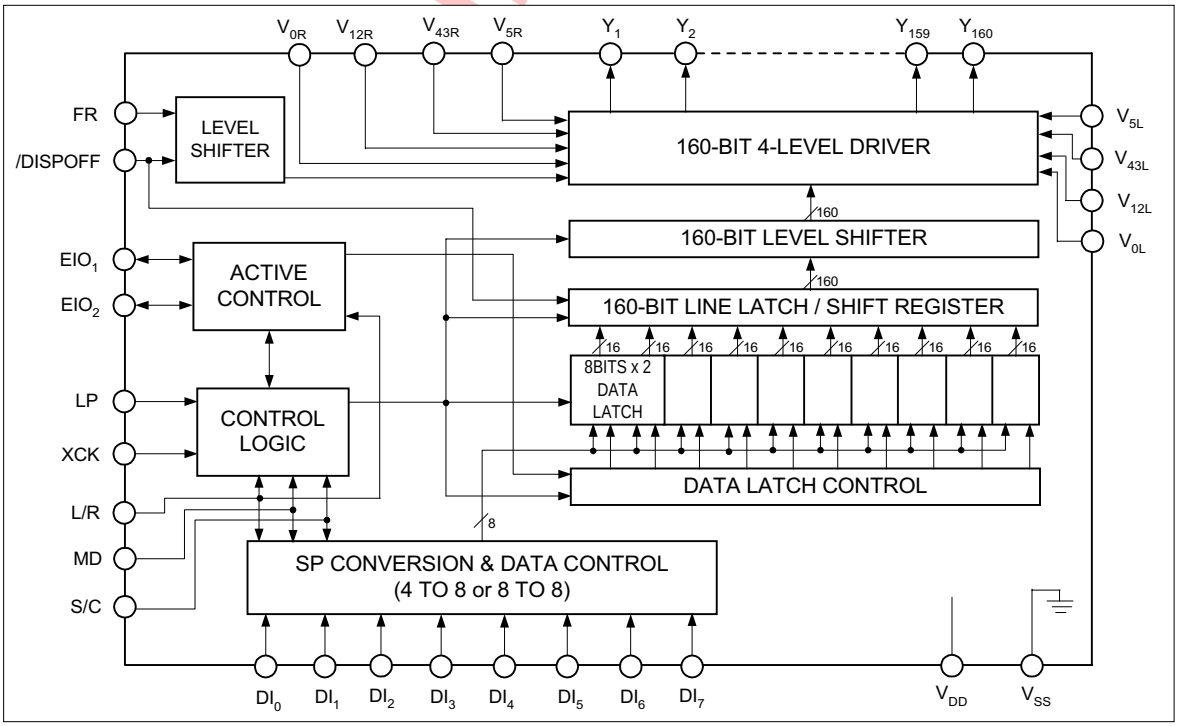
(Common mode)

- Shift clock frequency：4 MHz(MAX.)
- Built-in 160-bit bi-directional shift register (divisible into 80 bits x 2)
- Available in a single mode(160-bit shift register) or in a dual mode(80-bit shift register x 2)

(1) $Y_1 \rightarrow Y_{160}$ Single mode
(2) $Y_{160} \rightarrow Y_1$ Single mode
(3) $Y_1 \rightarrow Y_{80}$, $Y_{81} \rightarrow Y_{160}$ Dual mode
(4) $Y_{160} \rightarrow Y_{81}$, $Y_{80} \rightarrow Y_1$ Dual mode
The above 4 shift directions are pin-selectable

- Shift register circuits are reset when /DISPOFF active

BLOCK DIAGRAM



FUNCTIONAL OPERATIONS OF EACH BLOCK

BLOCK	FUNCTION
Active Control	In case of segment mode, controls the selection or non-selection of chip. Following an LP signal input, and after the chip selection signal is input, a selection signal is generated internally until 160 bits of data have been read in. Once data input has been completed, a selection signal for cascade connection is output, and the chip is non-selected. In case of common mode, controls the input/output data of bi-directional pins.
SP Conversion & Data Control	In case of segment mode, keeps input data which are 2 clocks of XCK at 4-bit parallel Input mode in latch circuit, or keeps input data which are 1 clock of XCK at 8-bit parallel Input mode in latch circuit; after that they are put on the internal data bus 8 bits at a time.
Data Latch Control	In case of segment mode, selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic. For every 16 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.
Data Latch	In case of segment mode, latches the data on the data bus. The latch state of each LCD drive output pin is controlled by the control logic and the data latch control; 160 bits of data are read in 20 sets of 8 bits.
Line Latch/ Shift Register	In case of segment mode, all 160 bits which have been read into the data latch are simultaneously latched at the falling edge of the LP signal, and are output to the level shifter block. In case of common mode, shifts data from the data input pin at the falling edge of the LP signal.
Level Shifter	The logic voltage signal is level-shifted to the LCD drive voltage level, and is output to the driver block.
4-Level Driver	Drives the LCD drive output pins from the line latch/shift register data, and selects one of 4 levels (V_0, V_{12},V_{43}, or V_5) based on the S/C, FR and /DISPOFF signals.
Control Logic	Controls the operation of each block. In case of segment mode, when an LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission is controlled, 160 bits of data are read in, and the chip is non-selected. In case of common mode, controls the direction of data shift.

PIN DESCRIPTION

SYMBOL	I/O	DESCRIPTION
$Y_1 \rightarrow Y_{160}$	O	LCD drive output
V_{0L}, V_{0R}	-	Power supply for LCD drive
V_{12L}, V_{12R}	-	Power supply for LCD drive
V_{43L}, V_{43R}	-	Power supply for LCD drive
V_{5L}, V_{5R}	-	Power supply for LCD drive
L/R	I	Input for selecting the reading direction of display data at segment mode/ Input for selecting the shift direction of shift register at common mode
V_{DD}	-	Power supply for logic system (+2.5 to +5.5 V)
S/C	I	Segment mode/common mode selection
EIO_2, EIO_1	I/O	Input/output for chip selection at segment mode/ Shift data input/output for shift register at common mode
DI_0-DI_6	I	Display data input at segment mode
DI_7	I	Display data input at segment mode/Dual mode data input at common mode
XCK	I	Clock input for taking display data at segment mode
/DISPOFF	I	Control input for output of non-select level
LP	I	Latch pulse input for display data at segment mode/ Shift clock input for shift register at common mode
FR	I	AC-converting signal input for LCD drive waveform
MD	I	Mode selection input
V_{SS}	-	Ground (0 V)

FUNCTIONAL DESCRIPTION

Pin Functions

(Segment mode)

SYMBOL	FUNCTION
V_{DD}	Logic system power supply pin, connected to +2.5 to +5.5 V.
V_{SS}	Ground pin, connected to 0 V.
V_{0L}, V_{0R} V_{12L}, V_{12R} V_{43L}, V_{43R} V_{5L}, V_{5R}	Bias power supply pins for LCD drive voltage • Normally use the bias voltages set by a resistor divider • Ensure that voltages are set such that $V_{SS} \le V_5 < V_{43} < V_{12} < V_0$.
DI_7-DI_0	Input pins for display data • In 4-bit parallel input mode, input data into the 4 pins, DI_3-DI_0. Connect DI_7-DI_4 to V_{SS} or V_{DD}. • In 8-bit parallel input mode, input data into the 8 pins, DI_7-DI_0. • Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations.
XCK	Clock input pin for taking display data • Data is read at the falling edge of the clock pulse.
LP	Latch pulse input pin for display data • Data is latched at the falling edge of the clock pulse.
L/R	Input pin for selecting the reading direction of display data • When set to V_{SS} level "L", data is read sequentially from Y_{160} to Y_1. • When set to V_{DD} level "H", data is read sequentially from Y_1 to Y_{160}. • Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations.
/DISPOFF	Control input pin for output of non-select level • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to V_{SS} level "L", the LCD drive output pins (Y_1-Y_{160}) are set to level V_5. • When set to "L", the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of /DISPOFF. When the /DISPOFF function is canceled, the driver outputs non-select level (V_{12} or V_{43}), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, it can not output the reading data correctly. • Table of truth values is shown in "**TRUTH TABLE**" in Functional Operations.

(Segment mode continuous)

SYMBOL	FUNCTION
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal. • Table of truth values is shown in "**TRUTH TABLE**" in Functional Operations.
MD	Mode selection pin • When set to V_{SS} level "L", 4-bit parallel input mode is set. • When set to V_{DD} level "H", 8-bit parallel input mode is set. • Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations.
S/C	Segment mode/common mode selection pin • When set to V_{DD} level "H", segment mode is set.
EIO_I-EIO_2	Input/output pins for chip selection • When L/R input is at V_{SS} level "L", EIO_1 is set for output, and EIO_2 is set for input. • When L/R input is at V_{DD} level "H", EIO_1 is set for input, and EIO_2 is set for output. • During output, set to "H" while LP • /XCK is "H" and after 160 bits of data have been read, set to "L" for one cycle (from falling edge to falling edge of XCK), after which it returns to "H". • During input, the chip is selected while EI is set to "L" after the LP signal is input. The chip is non-selected after 160 bits of data have been read. (EI：When EIO_1,EIO_2 is set for input ; EO：When EIO_1,EIO_2 is set for output.) • Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations.
Y_I-Y_{I60}	LCD drive output pins • Corresponding directly to each bit of the data latch, one level (V_0, V_{12}, V_{43}, or V_5) is selected and output. • Table of truth values is shown in "**TRUTH TABLE**" in Functional Operations.

(Common mode)

SYMBOL	FUNCTION
V_{DD}	Logic system power supply pin, connected to +2.5 to +5.5 V.
V_{SS}	Ground pin, connected to 0 V.
V_{0L}, V_{0R} V_{12L}, V_{12R} V_{43L}, V_{43R} V_{5L}, V_{5R}	Bias power supply pins for LCD drive voltage • Normally use the bias voltages set by a resistor divider • Ensure that voltages are set such that $V_{SS} \le V_5 < V_{43} < V_{12} < V_0$.
EIO_I	Shift data input/output pin for bi-directional shift register • Output pin when L/R is at V_{SS} level "L", input pin when L/R is at V_{DD} level "H". • When L/R = H, EIO_1 is used as input pin, it will be pulled down. • When L/R = L, EIO_1 is used as output pin, it won't be pulled down. • Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations.
EIO_2	Shift data input/output pin for bi-directional shift register • Input pin when L/R is at V_{SS} level "L", output pin when L/R is at V_{DD} level "H". • When L/R = L, EIO_2 is used as input pin, it will be pulled down. • When L/R = H, EIO_2 is used as output pin, it won't be pulled down. • Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations.
LP	Shift clock pulse input pin for bi-directional shift register • Data is shifted at the falling edge of the clock pulse.
L/R	Input pin for selecting the shift direction of bi-directional shift register • Data is shifted from Y_{160} to Y_1 when set to V_{SS} level "L", and data is shifted from Y_1 to Y_{160} when set to V_{DD} level "H". • Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations.
/DISPOFF	Control input pin for output of non-select level • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to V_{SS} level "L", the LCD drive output pins (Y_1-Y_{160}) are set to level V_5. • When set to "L", the contents of the shift register are reset to not reading data. When the /DISPOFF function is canceled, the driver outputs non-select level (V_{12} or V_{43}), and the shift data is read at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, the data is not read correctly. • Table of truth values is shown in "**TRUTH TABLE**" in Functional Operations.

(Common mode continuous)

SYMBOL	FUNCTION
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal. • Table of truth values is shown in "**TRUTH TABLE**" in Functional Operations.
MD	Mode selection pin • When set to V_{SS} level "L", single mode is selected; when set to V_{DD} level "H", dual mode is selected • Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations.
DI_7	Dual mode data input pin • According to the data shift direction of the data shift register, data can be input starting from the 81st bit. When the chip is used in dual mode, DI_7 will be pulled down. When the chip is used in single mode, DI_7 won't be pulled down. • Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations.
S/C	Segment mode/common mode selection pin • When set to V_{SS} level "L", common mode is set.
DI_6-DI_0	Not used • Connect DI6-DI0 to V_{SS} or V_{DD}, avoiding floating.
XCK	Not used • XCK is pulled down in common mode, so connect to V_{SS} or open.
Y_I-Y_{I60}	LCD drive output pins • Corresponding directly to each bit of the shift register, one level (V_0, V_{12}, V_{43}, or V_5) is selected and output. • Table of truth values is shown in "**TRUTH TABLE**" in Functional Operations.

Functional Operations

TRUTH TABLE

(Segment Mode)

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (Y_1-Y_{160})
L	L	H	V_{43}
L	H	H	V_5
H	L	H	V_{12}
H	H	H	V_0
X	X	L	V_5

(Common Mode)

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (Y_1-Y_{160})
L	L	H	V_{43}
L	H	H	V_0
H	L	H	V_{12}
H	H	H	V_5
X	X	L	V_5

NOTES :

- $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$, L : V_{SS} (0 V), H : V_{DD} (+2.5 to +5.5 V), X : Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.

There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver.

Supply regular voltage which is assigned by specification for each power pin.

RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS

(Segment Mode)

(a) 4-bit Parallel Input Mode

MD	L/R	EIO_1	EIO_2	DATA INPUT	NUMBER OF CLOCKS						
					40 CLOCK	39 CLOCK	38 CLOCK	...	3 CLOCK	2 CLOCK	1 CLOCK
L	L	Output	Input	DI_0	Y_1	Y_5	Y_9	...	Y_{149}	Y_{153}	Y_{157}
				DI_1	Y_2	Y_6	Y_{10}	...	Y_{150}	Y_{154}	Y_{158}
				DI_2	Y_3	Y_7	Y_{11}	...	Y_{151}	Y_{155}	Y_{159}
				DI_3	Y_4	Y_8	Y_{12}	...	Y_{152}	Y_{156}	Y_{160}
L	H	Input	Output	DI_0	Y_{160}	Y_{156}	Y_{152}	...	Y_{12}	Y_8	Y_4
				DI_1	Y_{159}	Y_{155}	Y_{151}	...	Y_{11}	Y_7	Y_3
				DI_2	Y_{158}	Y_{154}	Y_{150}	...	Y_{10}	Y_6	Y_2
				DI_3	Y_{157}	Y_{153}	Y_{149}	...	Y_9	Y_5	Y_1

(b) 8-bit Parallel Input Mode

MD	L/R	EIO_1	EIO_2	DATA INPUT	NUMBER OF CLOCKS						
					20 CLOCK	19 CLOCK	18 CLOCK	...	3 CLOCK	2 CLOCK	1 CLOCK
H	L	Output	Input	DI_0	Y_1	Y_9	Y_{17}	...	Y_{137}	Y_{145}	Y_{153}
				DI_1	Y_2	Y_{10}	Y_{18}	...	Y_{138}	Y_{146}	Y_{154}
				DI_2	Y_3	Y_{11}	Y_{19}	...	Y_{139}	Y_{147}	Y_{155}
				DI_3	Y_4	Y_{12}	Y_{20}	...	Y_{140}	Y_{148}	Y_{156}
				DI_4	Y_5	Y_{13}	Y_{21}	...	Y_{141}	Y_{149}	Y_{157}
				DI_5	Y_6	Y_{14}	Y_{22}	...	Y_{142}	Y_{150}	Y_{158}
				DI_6	Y_7	Y_{15}	Y_{23}	...	Y_{143}	Y_{151}	Y_{159}
				DI_7	Y_8	Y_{16}	Y_{24}	...	Y_{144}	Y_{152}	Y_{160}
H	H	Input	Output	DI_0	Y_{160}	Y_{152}	Y_{144}	...	Y_{24}	Y_{16}	Y_8
				DI_1	Y_{159}	Y_{151}	Y_{143}	...	Y_{23}	Y_{15}	Y_7
				DI_2	Y_{158}	Y_{150}	Y_{142}	...	Y_{22}	Y_{14}	Y_6
				DI_3	Y_{157}	Y_{149}	Y_{141}	...	Y_{21}	Y_{13}	Y_5
				DI_4	Y_{156}	Y_{148}	Y_{140}	...	Y_{20}	Y_{12}	Y_4
				DI_5	Y_{155}	Y_{147}	Y_{139}	...	Y_{19}	Y_{11}	Y_3
				DI_6	Y_{154}	Y_{146}	Y_{138}	...	Y_{18}	Y_{10}	Y_2
				DI_7	Y_{153}	Y_{145}	Y_{137}	...	Y_{17}	Y_9	Y_1

(Common Mode)

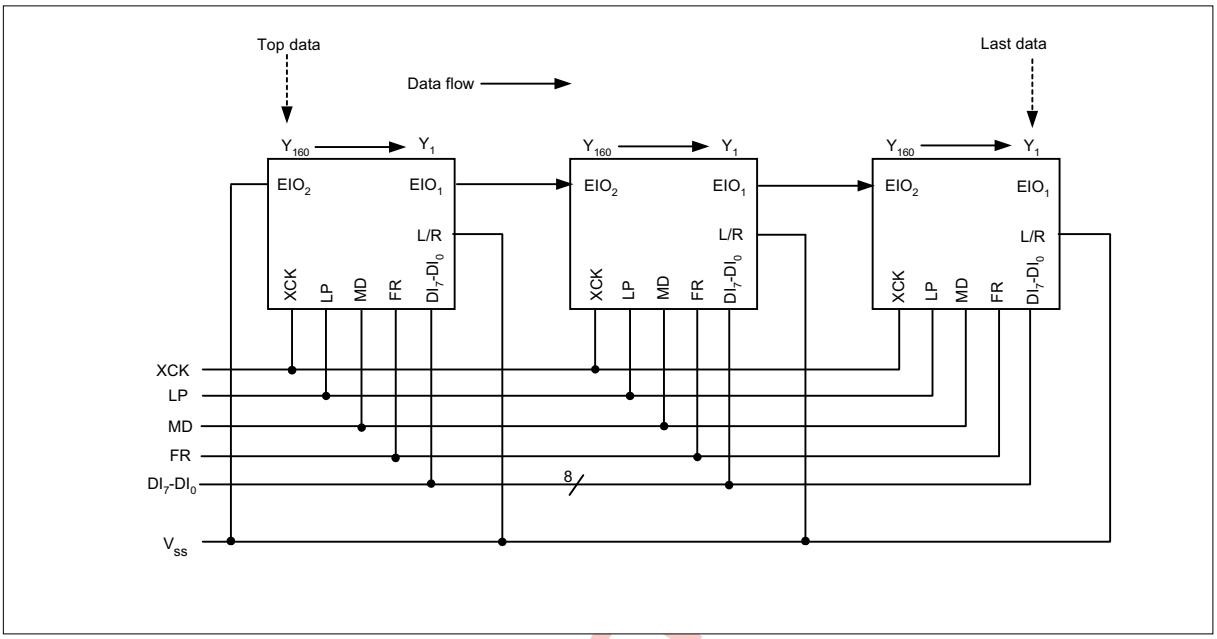
MD	L/R	DATA TRANSFER DIRECTION	EIO_1	EIO_2	DI_7
L (Single)	L	$Y_{160} \rightarrow Y_1$	Output	Input	X
	H	$Y_1 \rightarrow Y_{160}$	Input	Output	X
H (Dual)	L	$Y_{160} \rightarrow Y_{81}$ $Y_{80} \rightarrow Y_1$	Output	Input	Input
	H	$Y_1 \rightarrow Y_{80}$ $Y_{81} \rightarrow Y_{160}$	Input	Output	Input

NOTES :

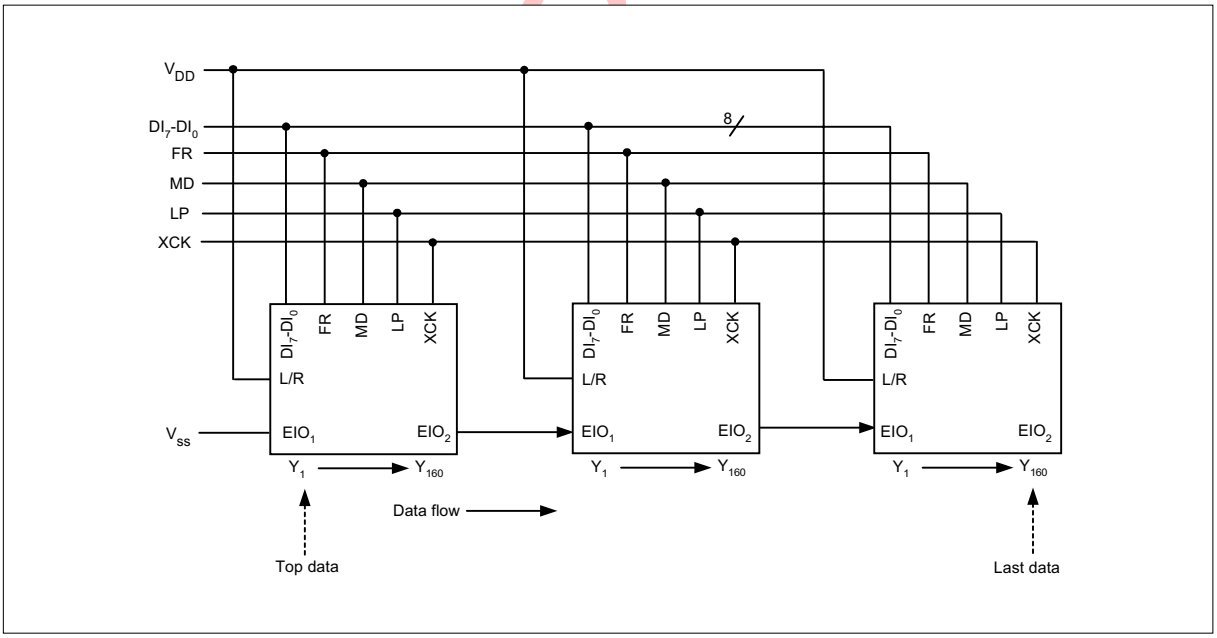
- L : V_{SS} (0 V), H : VDD(+2.5 to +5.5 V), X : Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.

CONNECTION EXAMPLES OF PLURAL SEGMENT DRIVERS

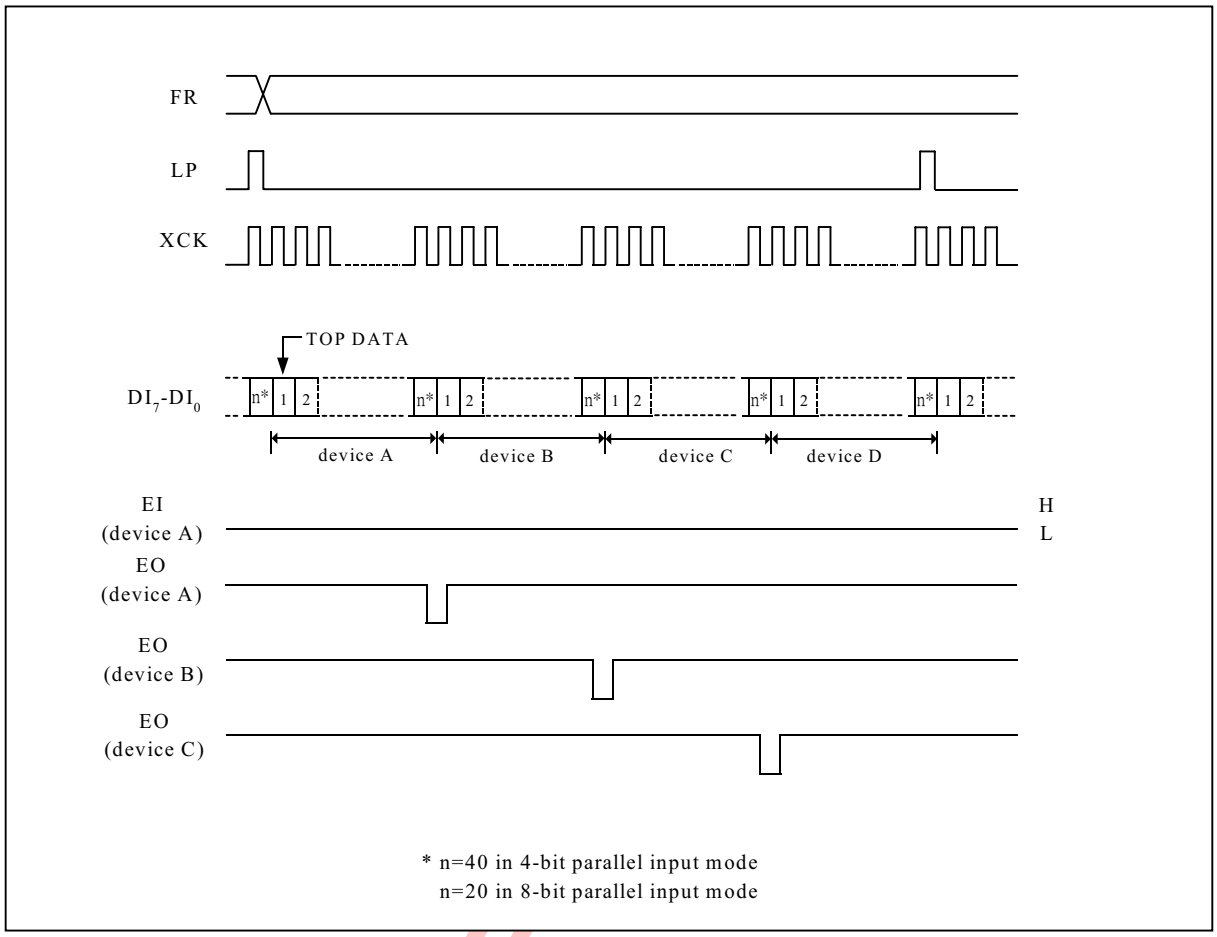
(a)When L/R= "L"



(b)When L/R= "H"



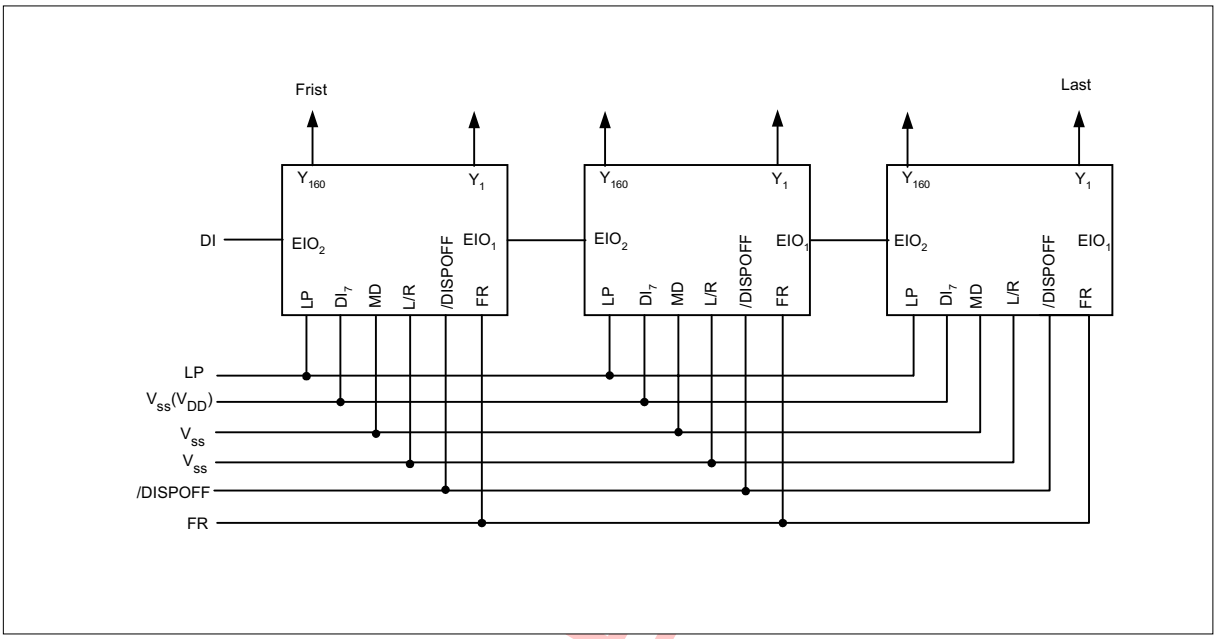
TIMING CHART OF 4-DEVICE CASCADE CONNECTION OF SEGMENT DRIVERS



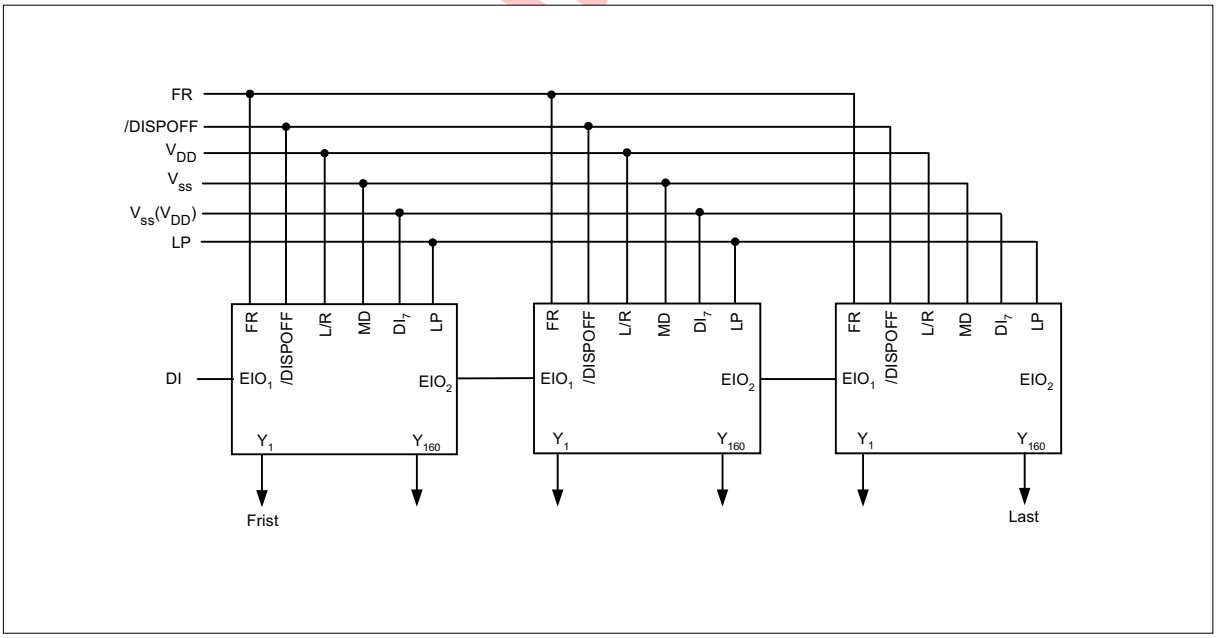
* n=40 in 4-bit parallel input mode
n=20 in 8-bit parallel input mode

CONNECTION EXAMPLES FOR PLURAL COMMON DRIVERS

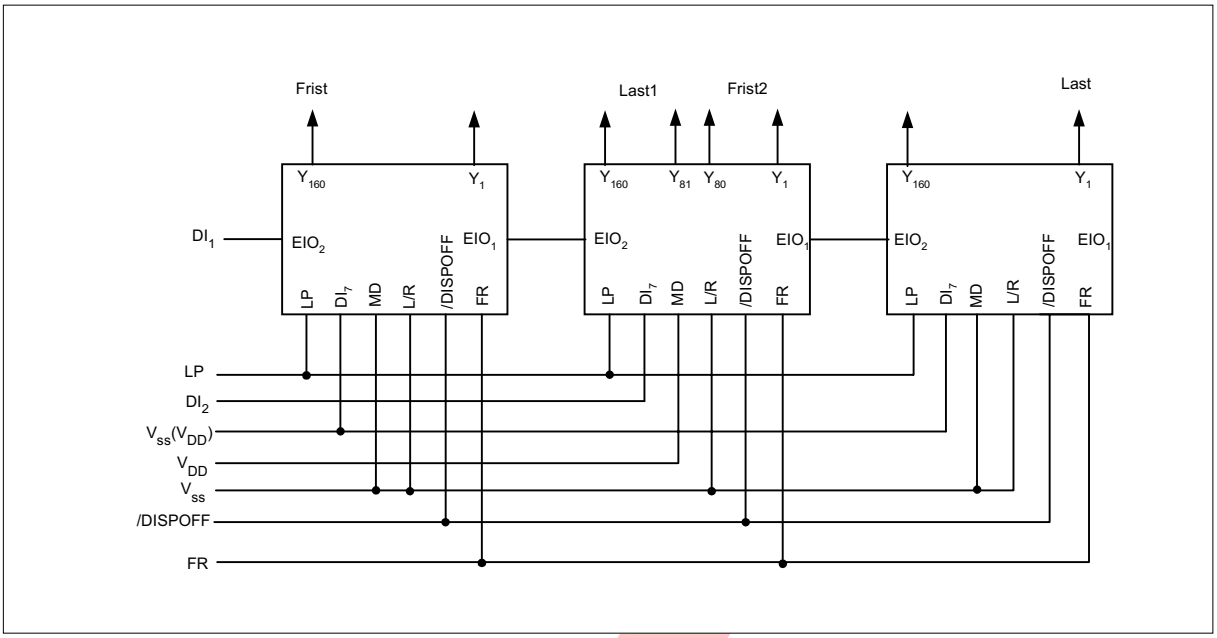
(a)Single Mode (L/R= “L”)



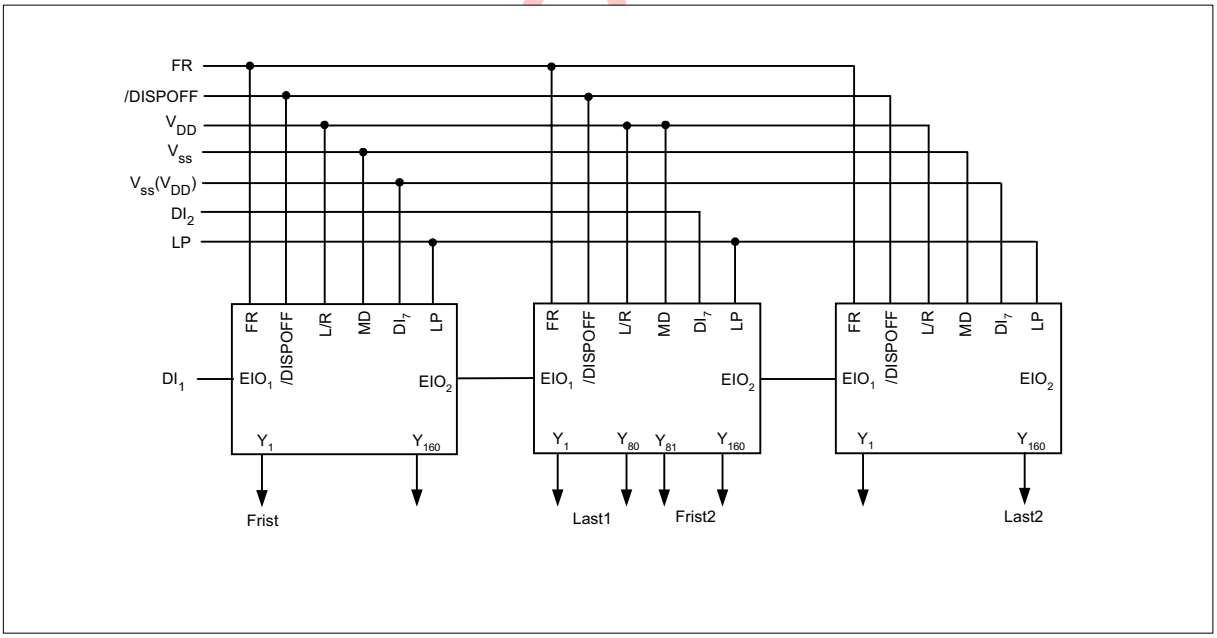
(b)Single Mode (L/R= “H”)



(c)Dual Mode (L/R= "L")



(d)Dual Mode (L/R= "H")



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	-0.3 to +7.0	V	1,2
Supply voltage (2)	V_0	V_{0L}, V_{0R}	-0.3 to +40.0	V	
	V_{12}	V_{12L}, V_{12R}	-0.3 to V0 +0.3	V	
	V_{43}	V_{43L}, V_{43R}	-0.3 to V0 +0.3	V	
	V_5	V_{5L}, V_{5R}	-0.3 to V0 +0.3	V	
Input voltage	V_I	DI_0-DI_7, XCL, LP, FR, MD, S/C, EIO_1, EIO_2, /DISPOFF	-0.3 to VDD +0.3	V	
Storage temperature	T_{STG}		-45 to +125	℃	

NOTES :

1. TA= +25 ℃

2. The maximum applicable voltage on any pin with respect to V_{SS} (0 V).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	+2.5		+5.5	V	1,2
Supply voltage (2)	V_0	V_{0L}, V_{0R}	+10.0		+40.0	V	
Operating temperature	T_{OPR}		-30		+85	℃	

NOTES :

1. The applicable voltage on any pin with respect to V_{SS} (0 V).

2. Ensure that voltages are set such that $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Segment Mode) (V_{SS} = V_5 = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = +10.0 to +40.0 V, T_{OPR} = -30 to +85 ℃)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		DI_7-DI_0, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, /DISPOFF			$0.2V_{DD}$	V	
Input "High" voltage	V_{IH}			$0.8V_{DD}$			V	
Output "Low" voltage	V_{OL}	I_{OL}=+0.4 mA	EIO_1, EIO_2			+0.4	V	
Output "High" voltage	V_{OH}	I_{OH}=-0.4 mA		V_{DD}-0.4			V	
Input leakage current	I_{LIL}	V_I = V_{SS}	DI_7-DI_0, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, /DISPOFF			-10.0	μA	
	I_{LIH}	V_I = V_{DD}				+10.0	μA	
Output resistance	R_{ON}	$\lvert\Delta V_{ON}\rvert$ =0.5V, V_0=30V	Y_1-Y_{160}		1.0	1.5	KΩ	
		$\lvert\Delta V_{ON}\rvert$ =0.5V, V_0=20V			1.5	2.0		
Standby current	I_{STB}		V_{SS}			50.0	μA	1
Supply current (1) (Non-selection)	I_{DD1}		V_{DD}			2.0	mA	2
Supply current (2) (selection)	I_{DD2}		V_{DD}			7.0	mA	3
Supply current (3)	I_0		V_{0L}, V_{0R}			0.9	mA	4

NOTES :

1. V_{DD} = +5.0 V, V_0 = +30.0 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}.
2. V_{DD} = +5.0 V, V_0 = +30.0 V, f_{XCK} = 8 MHz, no-load, EI = V_{DD}.
   The input data is turned over by data taking clock (4-bit parallel input mode).
3. V_{DD} = +5.0 V, V_0 = +30.0 V, f_{XCK} = 8 MHz, no-load, EI = V_{SS}.
   The input data is turned over by data taking clock (4-bit parallel input mode).
4. V_{DD} = +5.0 V, V_0 = +30.0 V, f_{XCK} = 8 MHz, f_{LP} = 19.2 kHz, f_{FR} = 80 Hz, no-load.
   The input data is turned over by data taking clock (4-bit parallel input mode).

(Common Mode) (V_{SS}= V_5= 0 V, V_{DD}= +2.5 to +5.5 V, V_0= +10.0 to +40.0 V, T_{OPR}= -30 to +85 ℃)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		DI_7-DI_0, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, /DISPOFF			0.2V_{DD}	V	
Input "High" voltage	V_{IH}			0.8V_{DD}			V	
Output "Low" voltage	V_{OL}	I_{OL}=+0.4 mA	EIO_1, EIO_2			+0.4	V	
Output "High" voltage	V_{OH}	I_{OH}=-0.4 mA		V_{DD}-0.4			V	
Input leakage current	I_{LIL}	V_I = V_{SS}	DI_7-DI_0, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, /DISPOFF			-10.0	μA	
	I_{LIH}	V_I = V_{DD}	DI_6-DI_0, LP, L/R, FR, MD, S/C, /DISPOFF			+10.0	μA	
Input pull-down current	I_{PD}	V_I = V_{DD}	DI_7, XCK, EIO_1, EIO_2			100.0	μA	3
						200.0	μA	4
Output resistance	R_{ON}	$\lvert\Delta V_{ON}\rvert$ =0.5V, V_0=30V	Y_1-Y_{160}		1.0	1.5	KΩ	
		$\lvert\Delta V_{ON}\rvert$ =0.5V, V_0=20V			1.5	2.0		
Standby current	I_{STB}		V_{SS}			50.0	μA	1
Supply current (1)	I_{DD}		V_{DD}			80.0	μA	2
Supply current (2)	I_0		V_{0L}, V_{0R}			130.0	μA	2

NOTES :

1. V_{DD} = +5.0 V, V_0 = +30.0 V, V_I = V_{SS}
2. V_{DD} = +5.0 V, V_0 = +30.0 V, f_{LP} = 19.2 kHz, f_{FR} = 80 Hz, 1/240 duty operation, no-load.
3. V_{DD}= +2.5 to +3.3 V
4. V_{DD}= +3.3 to +5.5 V

AC Characteristics

(Segment Mode) (V_{SS} = V_5 = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = +10.0 to +40.0 V, T_{OPR} = -30 to +85 ℃)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R, t_F≤ 11 ns	125			ns	1
Shift clock "H" pulse width	t_{WCKH}		51			ns	
Shift clock "L" pulse width	t_{WCKL}		51			ns	
Data setup time	t_{DS}		30			ns	
Data hold time	t_{DH}		40			ns	
Latch pulse "H" pulse width	t_{WLPH}		51			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		51			ns	
Latch pulse rise to shift clock rise time	t_{LS}		51			ns	
Latch pulse fall to shift clock fall time	t_{LH}		51			ns	
Enable setup time	t_S		36			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
/DISPOFF removal time	t_{SD}		100			ns	
/DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	C_L= 15 pF			78	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	C_L= 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	C_L= 15 pF			1.2	µs	

NOTES :

1. Takes the cascade connection into consideration.
2. (t_{WCK}- t_{WCKH}- t_{WCKL})/2 is maximum in the case of high speed operation.

Timing Chart of Segment Mode

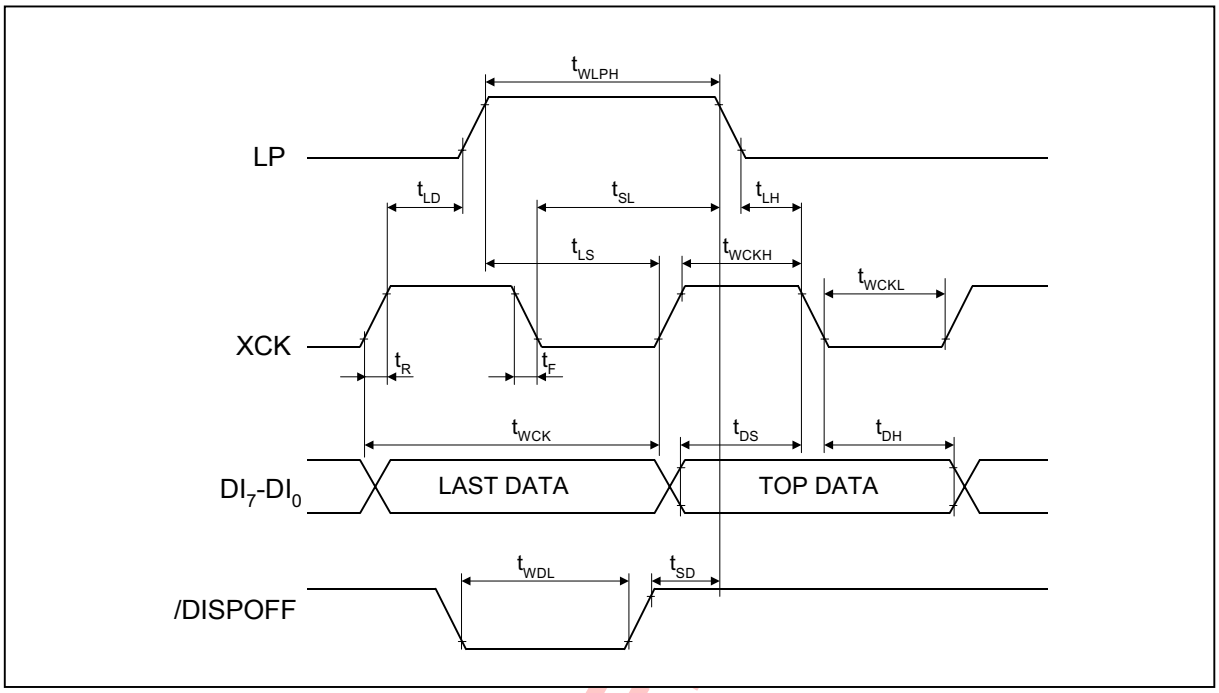


Fig.6 Timing Characteristics (1)

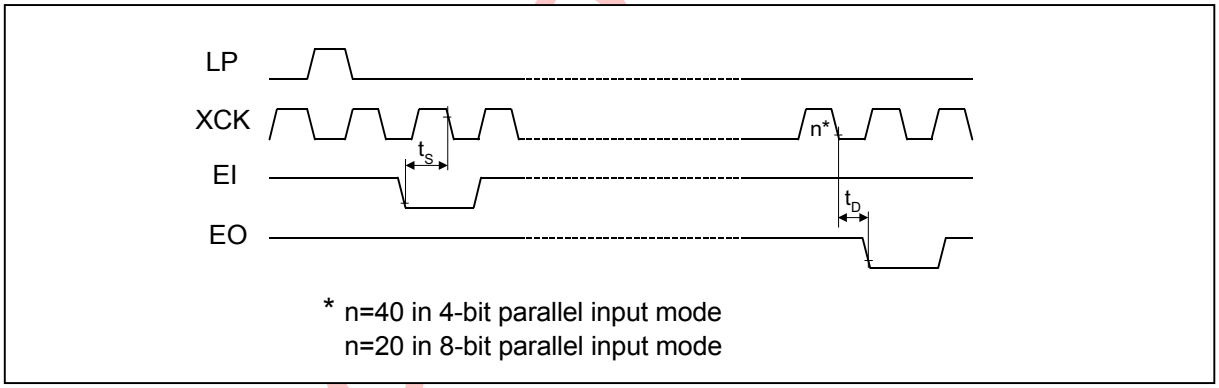


Fig.7 Timing Characteristics (2)

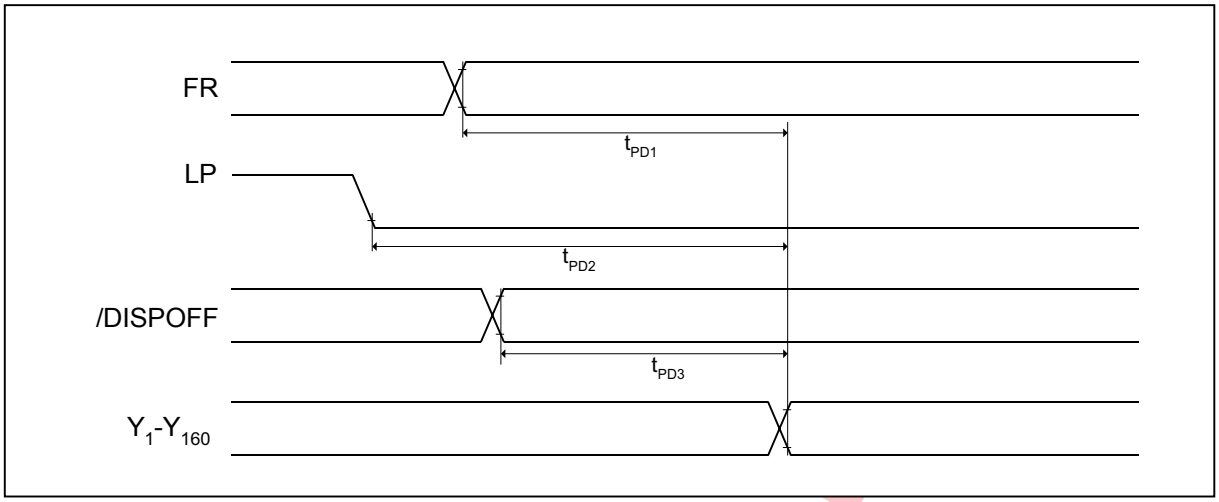
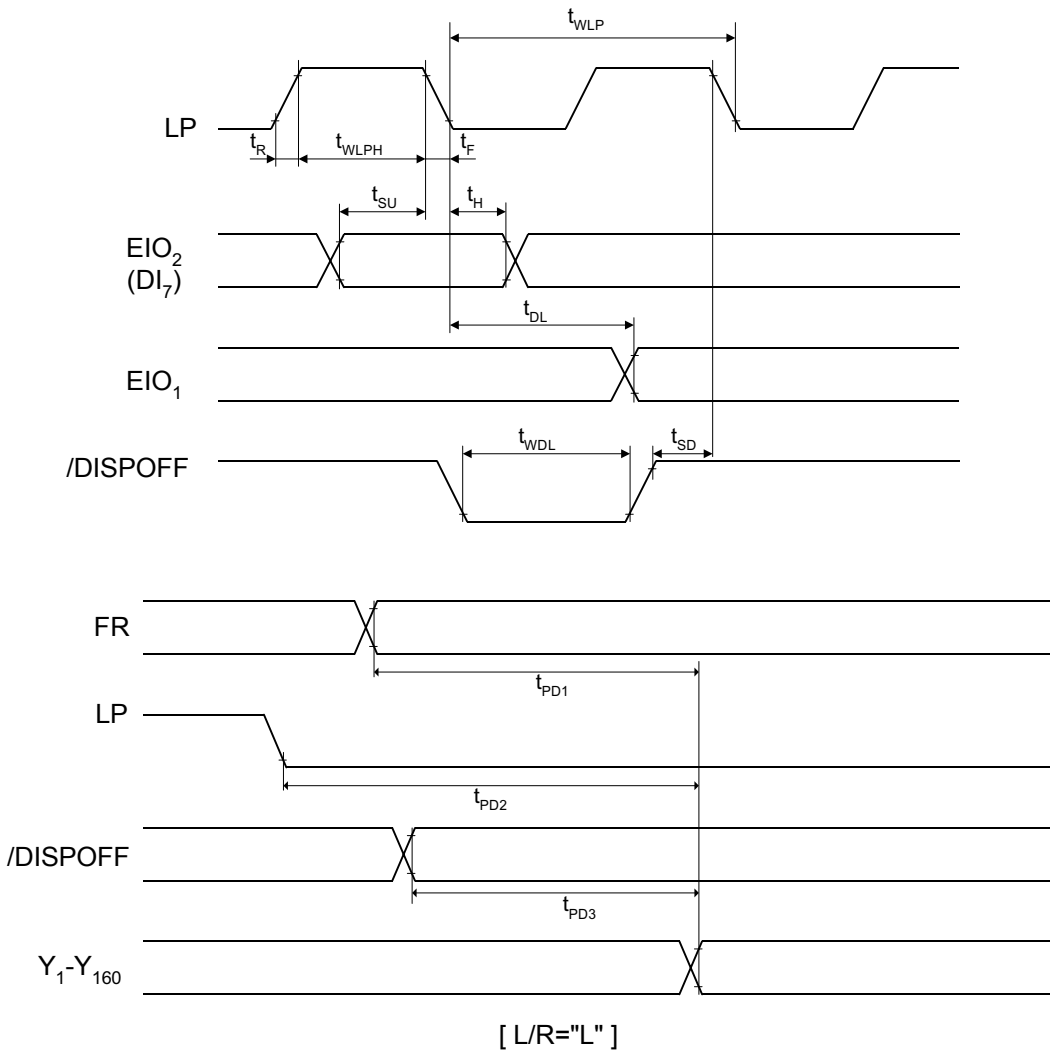


Fig.8 Timing Characteristics(3)

(Common Mode) (V_{SS} = V_5 = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = +10.0 to +40 V, T_{OPR} = -30 to +85 ℃)

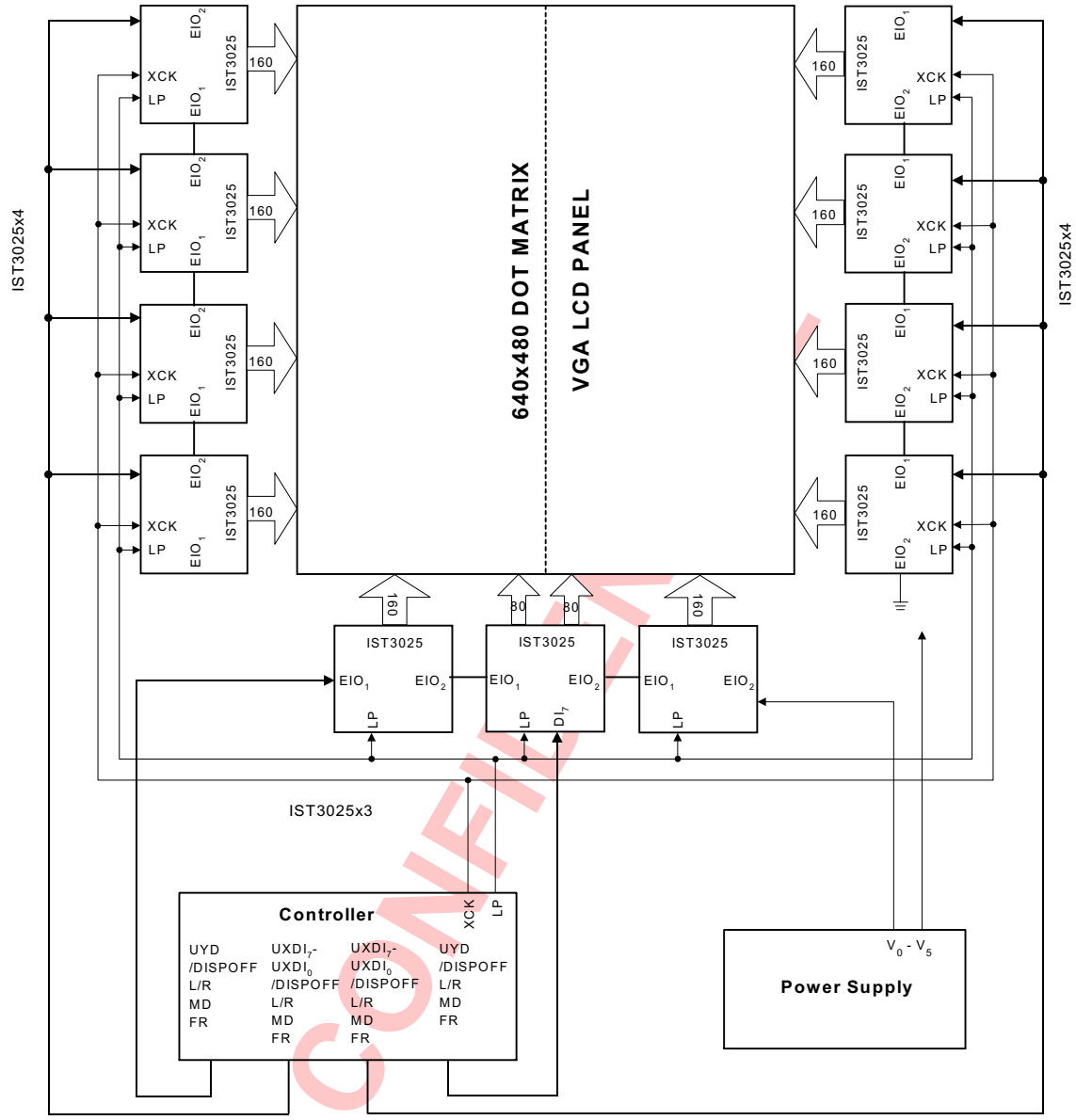
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Shift clock period	t_{WLP}	t_R, t_F≤ 20 ns	250			ns
Shift clock "H" pulse width	t_{WLPH}	V_{DD} = +5.0 ± 0.5V	15			ns
		V_{DD} = +2.5 to + 4.5V	30			ns
Data setup time	t_{SU}		30			ns
Data hold time	t_H		50			ns
Input signal rise time	t_R				50	ns
Input signal fall time	t_F				50	ns
/DISPOFF removal time	t_{SD}		100			ns
/DISPOFF "L" pulse width	T_{WDL}		1.2			µs
Output delay time (1)	t_{DL}	C_L= 15 pF			200	ns
Output delay time (2)	t_{PD1}, t_{PD2}	C_L= 15 pF			1.2	µs
Output delay time (3)	t_{PD3}	C_L= 15 pF			1.2	µs

Timing Chart of Common Mode



[L/R="L"]

SYSTEM CONFIGURATION EXAMPLE



PRECAUTIONS

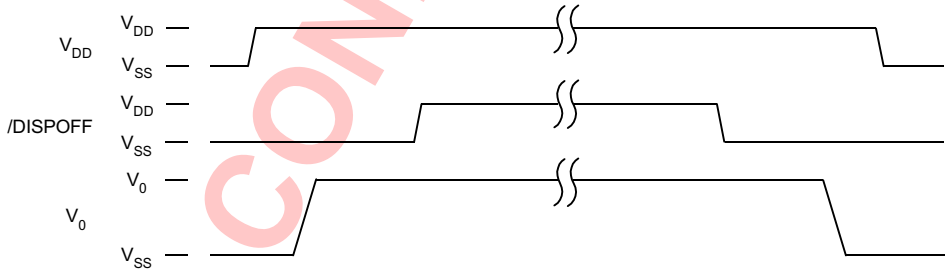
Precautions when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. The details are as follows.

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power.
- It is advisable to connect the serial resistor (50 to 100 Ω) or fuse to the LCD drive power V_0 of the system as a current limiter. Set up a suitable value of the resistor in consideration of the display grade.

And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on /DISPOFF function. After that, cancel the /DISPOFF function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level V_5 on /DISPOFF function. Then, disconnect the logic system power after disconnecting the LCD drive power.

When connecting the power supply, follow the recommended sequence shown here.



PAD CONFIGURATION :

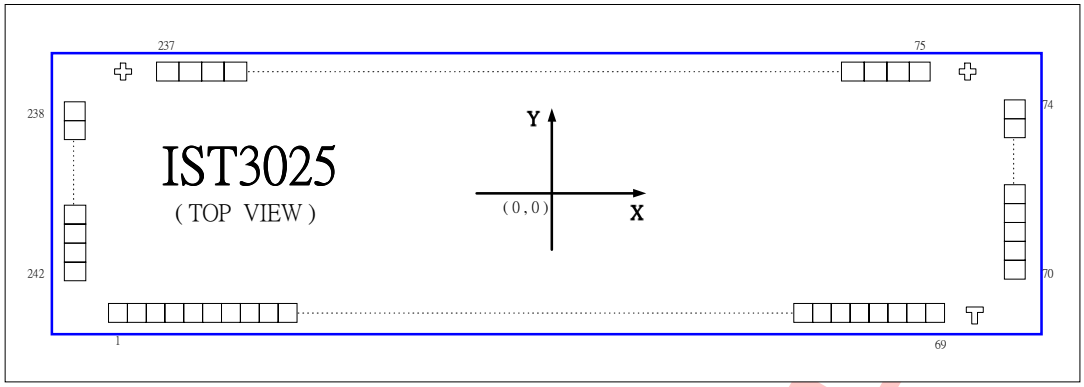
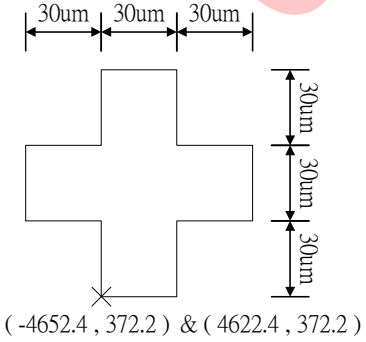


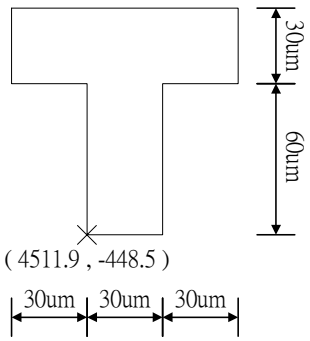
Figure 1 : IST3025 Chip Configuration

Table 1. IST3025 Pad Dimensions ※Note: All dummy pads have gold bumps.

Item	Pad No.	Size		Unit
		X	Y	
Chip size	242	9540	1080	um
Pad pitch	1 to 74, 238 to 242	100 (min)		
	75 to 237	55 (min)		
Bumped pad size	1 to 3, 64 to 69,	61	85	
	75,237	61	83	
	4 to 18, 58 to 63,	37	85	
	76 to 236	37	83	
	19 to 57	79	37	
	70 to 74, 238 to 242	85	61	
Bumped pad height	All pad	18		

COG Align Key Coordinate





PAD CENTER COORDINATES :

Table 2 : Pad Center Coordinates

Unit : um

PAD NO.	PAD NAME	PAD COORDINATES X	PAD COORDINATES Y	PAD NO.	PAD NAME	PAD COORDINATES X	PAD COORDINATES Y
1	DUMMY	-4446.8	-406.2	36	DUMMY	321.9	-426.2
2	V5	-4296.4	-406.2	37	DUMMY	421.9	-426.2
3	VSS	-4072.4	-406.2	38	DUMMY	521.9	-426.2
4	L/R	-3903.2	-406.2	39	DUMMY	621.9	-426.2
5	VDD	-3711.2	-406.2	40	DUMMY	721.9	-426.2
6	SC	-3589.4	-406.2	41	DUMMY	821.9	-426.2
7	VSS	-3407.4	-406.2	42	DUMMY	921.9	-426.2
8	EIO2	-3285.6	-406.2	43	DUMMY	1021.9	-426.2
9	DI0	-3089.9	-406.2	44	DUMMY	1121.9	-426.2
10	DI1	-2925.3	-406.2	45	DUMMY	1221.9	-426.2
11	DI2	-2729.1	-406.2	46	DUMMY	1321.9	-426.2
12	DI3	-2564.5	-406.2	47	DUMMY	1421.9	-426.2
13	VSS	-2382.5	-406.2	48	DUMMY	1521.9	-426.2
14	DI4	-2260.7	-406.2	49	DUMMY	1621.9	-426.2
15	DI5	-2064.5	-406.2	50	DUMMY	1721.9	-426.2
16	DI6	-1899.9	-406.2	51	DUMMY	1821.9	-426.2
17	DI7	-1703.7	-406.2	52	DUMMY	1921.9	-426.2
18	XCK	-1539.1	-406.2	53	DUMMY	2021.9	-426.2
19	DUMMY	-1378.1	-426.2	54	DUMMY	2121.9	-426.2
20	DUMMY	-1278.1	-426.2	55	DUMMY	2221.9	-426.2
21	DUMMY	-1178.1	-426.2	56	DUMMY	2321.9	-426.2
22	DUMMY	-1078.1	-426.2	57	DUMMY	2421.9	-426.2
23	DUMMY	-978.1	-426.2	58	/DISPOFF	2578.5	-406.2
24	DUMMY	-878.1	-426.2	59	LP	2743.1	-406.2
25	DUMMY	-778.1	-426.2	60	EIO1	2938.8	-406.2
26	DUMMY	-678.1	-426.2	61	FR	3103.4	-406.2
27	DUMMY	-578.1	-426.2	62	VDD	3295.4	-406.2
28	DUMMY	-478.1	-426.2	63	MD	3417.2	-406.2
29	DUMMY	-378.1	-426.2	64	VSS	3566.8	-406.2
30	DUMMY	-278.1	-426.2	65	VSS	3758.6	-406.2
31	DUMMY	-178.1	-426.2	66	VSS	3873.4	-406.2
32	DUMMY	-78.1	-426.2	67	VSS	4104.2	-406.2
33	DUMMY	21.9	-426.2	68	V5	4268.0	-406.2
34	DUMMY	121.9	-426.2	69	DUMMY	4418.4	-406.2
35	DUMMY	221.9	-426.2	70	DUMMY	4640.0	-338.4

Table 2 : Pad Center Coordinates (Continued)

Unit : um

PAD NO.	PAD NAME	PAD COORDINATES X	PAD COORDINATES Y	PAD NO.	PAD NAME	PAD COORDINATES X	PAD COORDINATES Y
71	V43	4640.0	-180.4	106	Y31	2777.5	420.0
72	V12	4640.0	24.0	107	Y32	2722.5	420.0
73	V0	4640.0	241.2	108	Y33	2667.5	420.0
74	DUMMY	4640.0	325.2	109	Y34	2612.5	420.0
75	DUMMY	4499.5	420.0	110	Y35	2557.5	420.0
76	Y1	4427.5	420.0	111	Y36	2502.5	420.0
77	Y2	4372.5	420.0	112	Y37	2447.5	420.0
78	Y3	4317.5	420.0	113	Y38	2392.5	420.0
79	Y4	4262.5	420.0	114	Y39	2337.5	420.0
80	Y5	4207.5	420.0	115	Y40	2282.5	420.0
81	Y6	4152.5	420.0	116	Y41	2227.5	420.0
82	Y7	4097.5	420.0	117	Y42	2172.5	420.0
83	Y8	4042.5	420.0	118	Y43	2117.5	420.0
84	Y9	3987.5	420.0	119	Y44	2062.5	420.0
85	Y10	3932.5	420.0	120	Y45	2007.5	420.0
86	Y11	3877.5	420.0	121	Y46	1952.5	420.0
87	Y12	3822.5	420.0	122	Y47	1897.5	420.0
88	Y13	3767.5	420.0	123	Y48	1842.5	420.0
89	Y14	3712.5	420.0	124	Y49	1787.5	420.0
90	Y15	3657.5	420.0	125	Y50	1732.5	420.0
91	Y16	3602.5	420.0	126	Y51	1677.5	420.0
92	Y17	3547.5	420.0	127	Y52	1622.5	420.0
93	Y18	3492.5	420.0	128	Y53	1567.5	420.0
94	Y19	3437.5	420.0	129	Y54	1512.5	420.0
95	Y20	3382.5	420.0	130	Y55	1457.5	420.0
96	Y21	3327.5	420.0	131	Y56	1402.5	420.0
97	Y22	3272.5	420.0	132	Y57	1347.5	420.0
98	Y23	3217.5	420.0	133	Y58	1292.5	420.0
99	Y24	3162.5	420.0	134	Y59	1237.5	420.0
100	Y25	3107.5	420.0	135	Y60	1182.5	420.0
101	Y26	3052.5	420.0	136	Y61	1127.5	420.0
102	Y27	2997.5	420.0	137	Y62	1072.5	420.0
103	Y28	2942.5	420.0	138	Y63	1017.5	420.0
104	Y29	2887.5	420.0	139	Y64	962.5	420.0
105	Y30	2832.5	420.0	140	Y65	907.5	420.0

Table 2 : Pad Center Coordinates (Continued)

Unit : um

PAD NO.	PAD NAME	PAD COORDINATES X	PAD COORDINATES Y	PAD NO.	PAD NAME	PAD COORDINATES X	PAD COORDINATES Y
141	Y66	852.5	420.0	176	Y100	-1127.5	420.0
142	Y67	797.5	420.0	177	Y101	-1182.5	420.0
143	Y68	742.5	420.0	178	Y102	-1237.5	420.0
144	Y69	687.5	420.0	179	Y103	-1292.5	420.0
145	Y70	632.5	420.0	180	Y104	-1347.5	420.0
146	Y71	577.5	420.0	181	Y105	-1402.5	420.0
147	Y72	522.5	420.0	182	Y106	-1457.5	420.0
148	Y73	467.5	420.0	183	Y107	-1512.5	420.0
149	Y74	412.5	420.0	184	Y108	-1567.5	420.0
150	Y75	357.5	420.0	185	Y109	-1622.5	420.0
151	Y76	302.5	420.0	186	Y110	-1677.5	420.0
152	Y77	247.5	420.0	187	Y111	-1732.5	420.0
153	Y78	192.5	420.0	188	Y112	-1787.5	420.0
154	Y79	137.5	420.0	189	Y113	-1842.5	420.0
155	Y80	82.5	420.0	190	Y114	-1897.5	420.0
156	DUMMY	0.0	420.0	191	Y115	-1952.5	420.0
157	Y81	-82.5	420.0	192	Y116	-2007.5	420.0
158	Y82	-137.5	420.0	193	Y117	-2062.5	420.0
159	Y83	-192.5	420.0	194	Y118	-2117.5	420.0
160	Y84	-247.5	420.0	195	Y119	-2172.5	420.0
161	Y85	-302.5	420.0	196	Y120	-2227.5	420.0
162	Y86	-357.5	420.0	197	Y121	-2282.5	420.0
163	Y87	-412.5	420.0	198	Y122	-2337.5	420.0
164	Y88	-467.5	420.0	199	Y123	-2392.5	420.0
165	Y89	-522.5	420.0	200	Y124	-2447.5	420.0
166	Y90	-577.5	420.0	201	Y125	-2502.5	420.0
167	Y91	-632.5	420.0	202	Y126	-2557.5	420.0
168	Y92	-687.5	420.0	203	Y127	-2612.5	420.0
169	Y93	-742.5	420.0	204	Y128	-2667.5	420.0
170	Y94	-797.5	420.0	205	Y129	-2722.5	420.0
171	Y95	-852.5	420.0	206	Y130	-2777.5	420.0
172	Y96	-907.5	420.0	207	Y131	-2832.5	420.0
173	Y97	-962.5	420.0	208	Y132	-2887.5	420.0
174	Y98	-1017.5	420.0	209	Y133	-2942.5	420.0
175	Y99	-1072.5	420.0	210	Y134	-2997.5	420.0

Table 2 : Pad Center Coordinates (Continued)

Unit : um

PAD NO.	PAD NAME	PAD COORDINATES X	PAD COORDINATES Y	PAD NO.	PAD NAME	PAD COORDINATES X	PAD COORDINATES Y
211	Y135	-3052.5	420.0				
212	Y136	-3107.5	420.0				
213	Y137	-3162.5	420.0				
214	Y138	-3217.5	420.0				
215	Y139	-3272.5	420.0				
216	Y140	-3327.5	420.0				
217	Y141	-3382.5	420.0				
218	Y142	-3437.5	420.0				
219	Y143	-3492.5	420.0				
220	Y144	-3547.5	420.0				
221	Y145	-3602.5	420.0				
222	Y146	-3657.5	420.0				
223	Y147	-3712.5	420.0				
224	Y148	-3767.5	420.0				
225	Y149	-3822.5	420.0				
226	Y150	-3877.5	420.0				
227	Y151	-3932.5	420.0				
228	Y152	-3987.5	420.0				
229	Y153	-4042.5	420.0				
230	Y154	-4097.5	420.0				
231	Y155	-4152.5	420.0				
232	Y156	-4207.5	420.0				
233	Y157	-4262.5	420.0				
234	Y158	-4317.5	420.0				
235	Y159	-4372.5	420.0				
236	Y160	-4427.5	420.0				
237	DUMMY	-4499.5	420.0				
238	DUMMY	-4640.0	325.2				
239	V0	-4640.0	241.2				
240	V12	-4640.0	24.0				
241	V43	-4640.0	-180.4				
242	DUMMY	-4640.0	-338.4				