Specification

Written by Department	Written by / Date	Approved by QRA Manager	Issued by D.C.C.
R&D	Charlie Cheng 2/04/2004	Joey Hsiao 2/06/2004	Kuo-wei Lee 2/06/2004

Controlled by DCC

Copy List

Code Name	100	200	300	400	500	600	700
Dept.	HR	S/M	MFG	R&D	CH	QRA	MIS
	--	--	--	✓	✓	✓	--

文件變更履歷頁

Document Change History

版次 Rev.	變更項次 Change Items#	變更內容簡述 Change Description	變更依據文件號碼 ECN #	生效日期 Eff. Date
001	-	New Release	E01030005	1/30/2003
002	Page1~31	配合進入正式量產(4/01/2003)階段,刪除各首頁之 Preliminary 字樣	E04030006	4/09/2003
003	Page01~0-2	Specification title :160 segment / common modify to 240 segment / common	E10030005	10/21/2003
004	Page 26	Bump pad size change	E02040002	2/06/2004

接續頁 CONTINUATION --- ■ 是 YES; □ 否 NO

IST3026

240-output LCD Segment/Common Driver IC

DESCRIPTION

The IST3026 is a 240-output segment/common driver IC suitable for driving medium size dot matrix LCD panels. The IST3026 is good both segment driver and common driver, and suitable for a low power consuming, high-precision LCD.

FEATURES

- Number of LCD drive outputs：240
- Supply voltage for the logic system：+2.5 to +5.5 V
- Supply voltage for LCD drive：+15.0 to + 40.0 V
- Low power consumption
- Low output impedance
- Operating temperature：-30 to +85 ℃
- Package：TCP (Tape Carrier Package) / Gold Bumped Chip

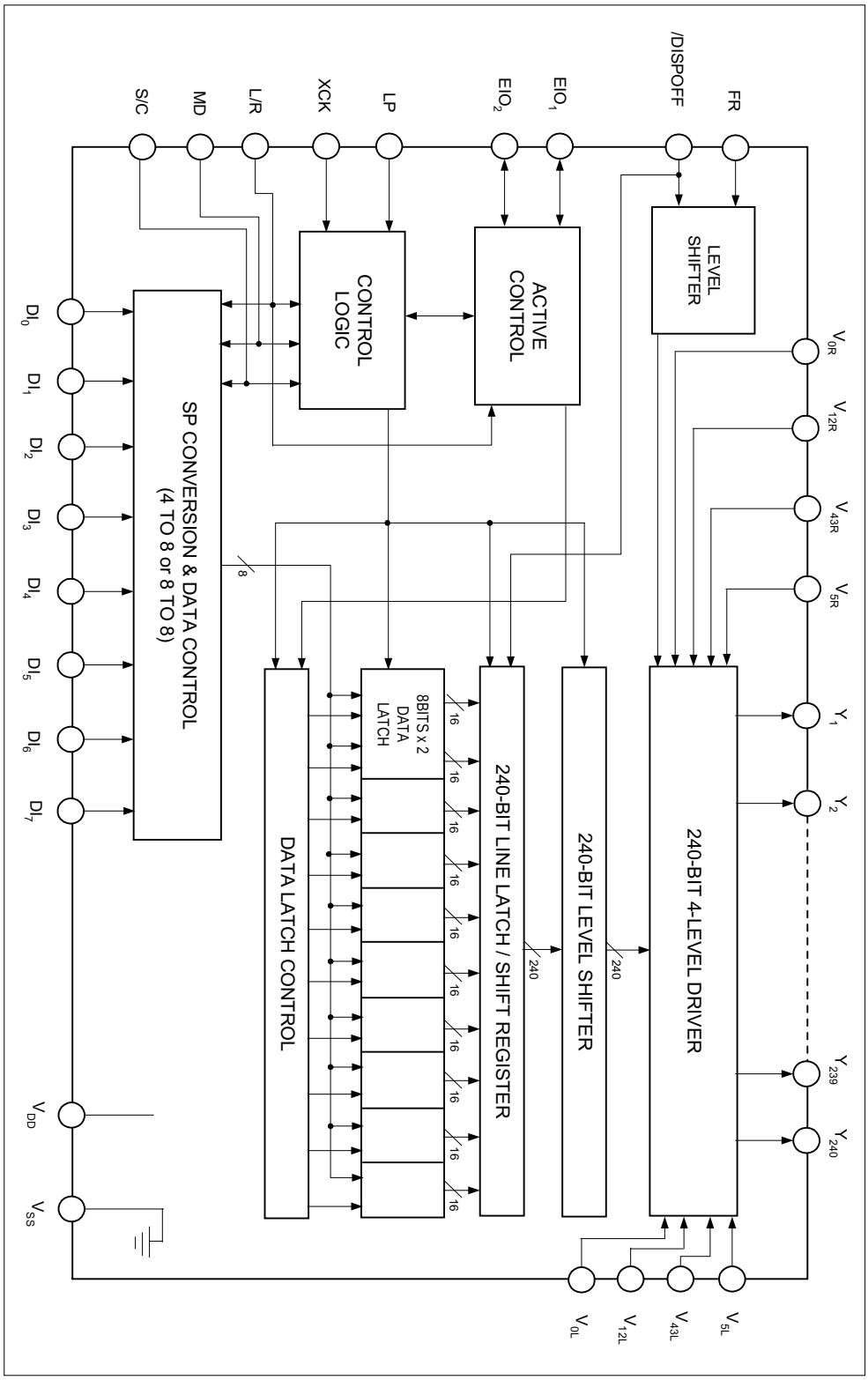
(Segment mode)

- Shift clock frequency
  - 20 MH_Z (MAX.)：V_{DD} = +5.0 ± 0.5 V
  - 15 MH_Z (MAX.)：V_{DD} = +3.0 to +4.5 V
  - 12 MH_Z (MAX.)：V_{DD} = +2.5 to +3.0 V
- 4-bit/8-bit parallel input modes are selectable with a mode (MD) pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 240 bits of input date
- Line latch circuits are reset when /DISPOFF active

(Common mode)

- Shift clock frequency：4 MHz (MAX.)
- Built-in 240-bit bi-directional shift register (divisible into 120 bits x 2)
- Available in a single mode (240-bit shift register) or in a dual mode (120-bit shift register x 2)
  (1) $Y_1 \rightarrow Y_{240}$ Single mode
  (2) $Y_{240} \rightarrow Y_1$ Single mode
  (3) $Y_1 \rightarrow Y_{120}$, $Y_{121} \rightarrow Y_{240}$ Dual mode
  (4) $Y_{240} \rightarrow Y_{121}$, $Y_{120} \rightarrow Y_1$ Dual mode
  The above 4 shift directions are pin-selectable
- Shift register circuits are reset when /DISPOFF active

BLOCK DIAGRAM



FUNCTIONAL OPERATIONS OF EACH BLOCK

BLOCK	FUNCTION
Active Control	In case of segment mode, controls the selection or non-selection of chip. Following an LP signal input, and after the chip selection signal is input , a selection signal is generated internally until 240 bits of data have been read in. Once data input has been completed, a selection signal for cascade connection is output, and the chip is non-selected. In case of common mode, controls the input/output data of bi-directional pins.
SP Conversion & Data Control	In case of segment mode, keeps input data which are 2 clocks of XCK at 4-bit parallel Input mode in latch circuit, or keeps input data which are 1 clock of XCK at 8-bit parallel Input mode in latch circuit; after that they are put on the internal data bus 8 bits at a time.
Data Latch Control	In case of segment mode, selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic. For every 16 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.
Data Latch	In case of segment mode, latches the data on the data bus. The latch state of each LCD drive output pin is controlled by the control logic and the data latch control; 240 bits of data are read in 30 sets of 8 bits.
Line Latch/ Shift Register	In case of segment mode, all 240 bits which have been read into the data latch are simultaneously latched at the falling edge of the LP signal, and are output to the level shifter block. In case of common mode, shifts data from the data input pin at the falling edge of the LP signal.
Level Shifter	The logic voltage signal is level-shifted to the LCD drive voltage level, and is output to the driver block.
4-Level Driver	Drives the LCD drive output pins from the line latch/shift register data, and selects one of 4 levels (V_0, V_{12},V_{43}, or V_5) based on the S/C, FR and /DISPOFF signals.
Control Logic	Controls the operation of each block. In case of segment mode, when an LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission is controlled, 240 bits of data are read in, and the chip is non-selected. In case of common mode, controls the direction of data shift.

PIN DESCRIPTION

SYMBOL	I/O	DESCRIPTION
$Y_1 \rightarrow Y_{120}$ $Y_{121} \rightarrow Y_{240}$	O	LCD drive output
V_{0L}, V_{0R}	-	Power supply for LCD drive
V_{12L}, V_{12R}	-	Power supply for LCD drive
V_{43L}, V_{43R}	-	Power supply for LCD drive
V_{5L}, V_{5R}	-	Power supply for LCD drive
V_{DD}	-	Power supply for logic system (+2.5 to +5.5 V)
S/C	I	Segment mode/common mode selection
EIO_2, EIO_1	I/O	Input/output for chip selection at segment mode/ Shift data input/output for shift register at common mode
DI_0-DI_6	I	Display data input at segment mode
DI_7	I	Display data input at segment mode/Dual mode data input at common mode
XCK	I	Clock input for taking display data at segment mode
/DISPOFF	I	Control input for output of non-select level
LP	I	Latch pulse input for display data at segment mode/ Shift clock input for shift register at common mode
FR	I	AC-converting signal input for LCD drive waveform
L/R	I	Input for selecting the reading direction of display data at segment mode/ Input for selecting the shift direction of shift register at common mode
MD	I	Mode selection input
V_{SS}	-	Ground (0 V)

FUNCTIONAL DESCRIPTION

Pin Functions

(Segment mode)

SYMBOL	FUNCTION
V_{DD}	Logic system power supply pin, connected to +2.5 to +5.5 V.
V_{SS}	Ground pin, connected to 0 V.
V_{0L}, V_{0R} V_{12L}, V_{12R} V_{43L}, V_{43R} V_{5L}, V_{5R}	Bias power supply pins for LCD drive voltage • Normally use the bias voltages set by a resistor divider • Ensure that voltages are set such that $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$.
DI_7-DI_0	Input pins for display data • In 4-bit parallel input mode, input data into the 4 pins, DI_3-DI_0. Connect DI_7-DI_4 to V_{SS} or V_{DD}. • In 8-bit parallel input mode, input data into the 8 pins, DI_7-DI_0. • Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations.
XCK	Clock input pin for taking display data • Data is read at the falling edge of the clock pulse.
LP	Latch pulse input pin for display data • Data is latched at the falling edge of the clock pulse.
L/R	Input pin for selecting the reading direction of display data • When set to V_{SS} level "L", data is read sequentially from Y_{240} to Y_1. • When set to V_{DD} level "H", data is read sequentially from Y_1 to Y_{240}. • Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations.
/DISPOFF	Control input pin for output of non-select level • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to V_{SS} level "L", the LCD drive output pins (Y_1-Y_{240}) are set to level V_5. • When set to "L", the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of /DISPOFF. When the /DISPOFF function is canceled, the driver outputs non-select level (V_{12} or V_{43}), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, it can not output the reading data correctly. • Table of truth values is shown in "**TRUTH TABLE**" in Functional Operations.

(Segment mode continuous)

SYMBOL	FUNCTION
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal. • Table of truth values is shown in "**TRUTH TABLE**" in Functional Operations.
MD	Mode selection pin • When set to V_{SS} level "L", 8-bit parallel input mode is set. • When set to V_{DD} level "H", 4-bit parallel input mode is set. • Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations.
S/C	Segment mode/common mode selection pin • When set to V_{DD} level "H", segment mode is set.
EIO_I-EIO_2	Input/output pins for chip selection • When L/R input is at V_{SS} level "L", EIO_1 is set for output, and EIO_2 is set for input. • When L/R input is at V_{DD} level "H", EIO_1 is set for input, and EIO_2 is set for output. • During output, set to "H" while LP • /XCK is "H" and after 240 bits of data have been read, set to "L" for one cycle (from falling edge to falling edge of XCK), after which it returns to "H". • During input, the chip is selected while EI is set to "L" after the LP signal is input. The chip is non-selected after 240 bits of data have been read. (EI：When EIO_1,EIO_2 is set for input ; EO：When EIO_1,EIO_2 is set for output.) • Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations.
Y_I-Y_{240}	LCD drive output pins • Corresponding directly to each bit of the data latch, one level (V_0, V_{12}, V_{43}, or V_5) is selected and output. • Table of truth values is shown in "**TRUTH TABLE**" in Functional Operations.

(Common mode)

SYMBOL	FUNCTION
V_{DD}	Logic system power supply pin, connected to +2.5 to +5.5 V.
V_{SS}	Ground pin, connected to 0 V.
V_{0L}, V_{0R} V_{12L}, V_{12R} V_{43L}, V_{43R} V_{5L}, V_{5R}	Bias power supply pins for LCD drive voltage • Normally use the bias voltages set by a resistor divider • Ensure that voltages are set such that $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$.
EIO_I	Shift data input/output pin for bi-directional shift register • Output pin when L/R is at V_{SS} level "L", input pin when L/R is at V_{DD} level "H". • When L/R = H, EIO_1 is used as input pin, it will be pulled down. • When L/R = L, EIO_1 is used as output pin, it won't be pulled down. • Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations.
EIO_2	Shift data input/output pin for bi-directional shift register • Input pin when L/R is at V_{SS} level "L", output pin when L/R is at V_{DD} level "H". • When L/R = L, EIO_2 is used as input pin, it will be pulled down. • When L/R = H, EIO_2 is used as output pin, it won't be pulled down. • Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations.
LP	Shift clock pulse input pin for bi-directional shift register • Data is shifted at the falling edge of the clock pulse.
L/R	Input pin for selecting the shift direction of bi-directional shift register • Data is shifted from Y_{240} to Y_1 when set to V_{SS} level "L", and data is shifted from Y_1 to Y_{240} when set to V_{DD} level "H". • Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations.
/DISPOFF	Control input pin for output of non-select level • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to V_{SS} level "L", the LCD drive output pins (Y_1-Y_{240}) are set to level V_5. • When set to "L", the contents of the shift register are reset to not reading data. When the /DISPOFF function is canceled, the driver outputs non-select level (V_{12} or V_{43}), and the shift data is read at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, the data is not read correctly. • Table of truth values is shown in "**TRUTH TABLE**" in Functional Operations.

(Common mode continuous)

SYMBOL	FUNCTION
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal. • Table of truth values is shown in "**TRUTH TABLE**" in Functional Operations.
MD	Mode selection pin • When set to V_{SS} level "L", single mode is selected; when set to V_{DD} level "H", dual mode is selected • Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations.
DI_7	Dual mode data input pin • According to the data shift direction of the data shift register, data can be input starting from the 121st bit. When the chip is used in dual mode, DI_7 will be pulled down. When the chip is used in single mode, DI_7 won't be pulled down. • Refer to "**RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS**" in Functional Operations.
S/C	Segment mode/common mode selection pin • When set to V_{SS} level "L", common mode is set.
DI_6-DI_0	Not used • Connect DI6-DI0 to V_{SS} or V_{DD}, avoiding floating.
XCK	Not used • XCK is pulled down in common mode, so connect to V_{SS} or open.
Y_1-Y_{240}	LCD drive output pins • Corresponding directly to each bit of the shift register, one level (V_0, V_{12}, V_{43}, or V_5) is selected and output. • Table of truth values is shown in "**TRUTH TABLE**" in Functional Operations.

Functional Operations

TRUTH TABLE

(Segment Mode)

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (Y_1-Y_{240})
L	L	H	V_{43}
L	H	H	V_5
H	L	H	V_{12}
H	H	H	V_0
X	X	L	V_5

(Common Mode)

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (Y_1-Y_{240})
L	L	H	V_{43}
L	H	H	V_0
H	L	H	V_{12}
H	H	H	V_5
X	X	L	V_5

NOTES :

- $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$, L : V_{SS} (0 V), H : V_{DD} (+2.5 to +5.5 V), X : Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.

There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver.

Supply regular voltage which is assigned by specification for each power pin.

RELATIONSHIP BETWEEN THE DISPLAY DATA AND LCD DRIVE OUTPUT PINS

(Segment Mode)

(a) 4-bit Parallel Input Mode

MD	L/R	EIO_1	EIO_2	DATA INPUT	NUMBER OF CLOCKS						
					60 CLOCK	59 CLOCK	58 CLOCK	...	3 CLOCK	2 CLOCK	1 CLOCK
H	L	Output	Input	DI_0	Y_1	Y_5	Y_9	...	Y_{229}	Y_{233}	Y_{237}
				DI_1	Y_2	Y_6	Y_{10}	...	Y_{230}	Y_{234}	Y_{238}
				DI_2	Y_3	Y_7	Y_{11}	...	Y_{231}	Y_{235}	Y_{239}
				DI_3	Y_4	Y_8	Y_{12}	...	Y_{232}	Y_{236}	Y_{240}
H	H	Input	Output	DI_0	Y_{240}	Y_{236}	Y_{232}	...	Y_{12}	Y_8	Y_4
				DI_1	Y_{239}	Y_{235}	Y_{231}	...	Y_{11}	Y_7	Y_3
				DI_2	Y_{238}	Y_{234}	Y_{230}	...	Y_{10}	Y_6	Y_2
				DI_3	Y_{237}	Y_{233}	Y_{229}	...	Y_9	Y_5	Y_1

(b) 8-bit Parallel Input Mode

MD	L/R	EIO_1	EIO_2	DATA INPUT	NUMBER OF CLOCKS						
					30 CLOCK	29 CLOCK	28 CLOCK	...	3 CLOCK	2 CLOCK	1 CLOCK
L	L	Output	Input	DI_0	Y_1	Y_9	Y_{17}	...	Y_{217}	Y_{225}	Y_{233}
				DI_1	Y_2	Y_{10}	Y_{18}	...	Y_{218}	Y_{226}	Y_{234}
				DI_2	Y_3	Y_{11}	Y_{19}	...	Y_{219}	Y_{227}	Y_{235}
				DI_3	Y_4	Y_{12}	Y_{20}	...	Y_{220}	Y_{228}	Y_{236}
				DI_4	Y_5	Y_{13}	Y_{21}	...	Y_{221}	Y_{229}	Y_{237}
				DI_5	Y_6	Y_{14}	Y_{22}	...	Y_{222}	Y_{230}	Y_{238}
				DI_6	Y_7	Y_{15}	Y_{23}	...	Y_{223}	Y_{231}	Y_{239}
				DI_7	Y_8	Y_{16}	Y_{24}	...	Y_{224}	Y_{232}	Y_{240}
L	H	Input	Output	DI_0	Y_{240}	Y_{232}	Y_{224}	...	Y_{24}	Y_{16}	Y_8
				DI_1	Y_{239}	Y_{231}	Y_{223}	...	Y_{23}	Y_{15}	Y_7
				DI_2	Y_{238}	Y_{230}	Y_{222}	...	Y_{22}	Y_{14}	Y_6
				DI_3	Y_{237}	Y_{229}	Y_{221}	...	Y_{21}	Y_{13}	Y_5
				DI_4	Y_{236}	Y_{228}	Y_{220}	...	Y_{20}	Y_{12}	Y_4
				DI_5	Y_{235}	Y_{227}	Y_{219}	...	Y_{19}	Y_{11}	Y_3
				DI_6	Y_{234}	Y_{226}	Y_{218}	...	Y_{18}	Y_{10}	Y_2
				DI_7	Y_{233}	Y_{225}	Y_{217}	...	Y_{17}	Y_9	Y_1

(Common Mode)

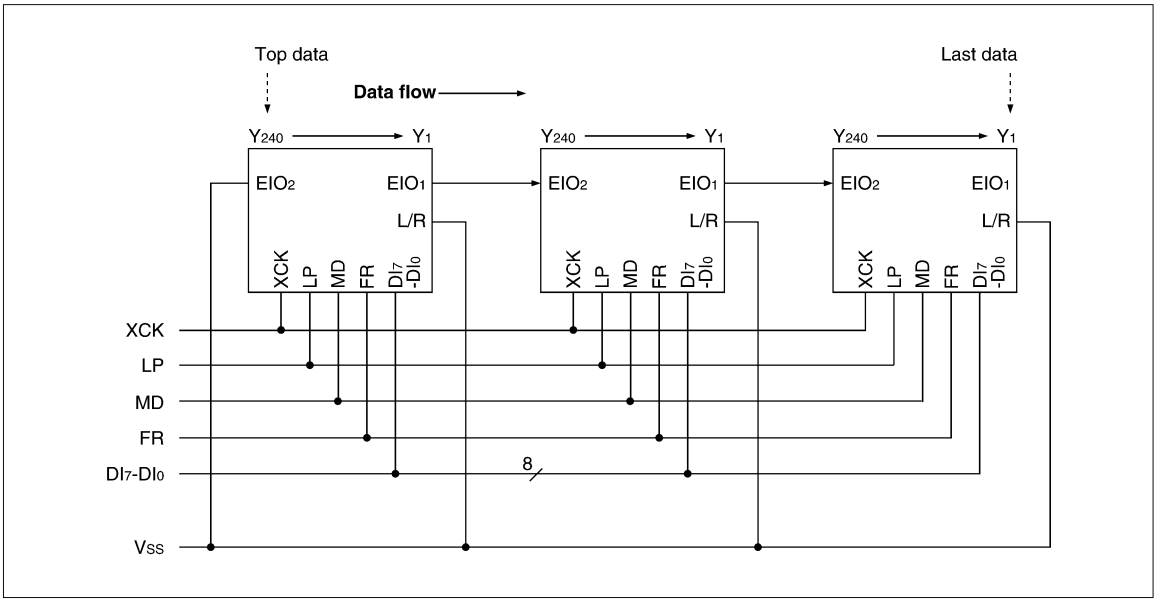
MD	L/R	DATA TRANSFER DIRECTION	EIO_1	EIO_2	DI_7
L (Single)	L	$Y_{240} \rightarrow Y_1$	Output	Input	X
	H	$Y_1 \rightarrow Y_{240}$	Input	Output	X
H (Dual)	L	$Y_{240} \rightarrow Y_{121}$ $Y_{120} \rightarrow Y_1$	Output	Input	Input
	H	$Y_1 \rightarrow Y_{120}$ $Y_{121} \rightarrow Y_{240}$	Input	Output	Input

NOTES :

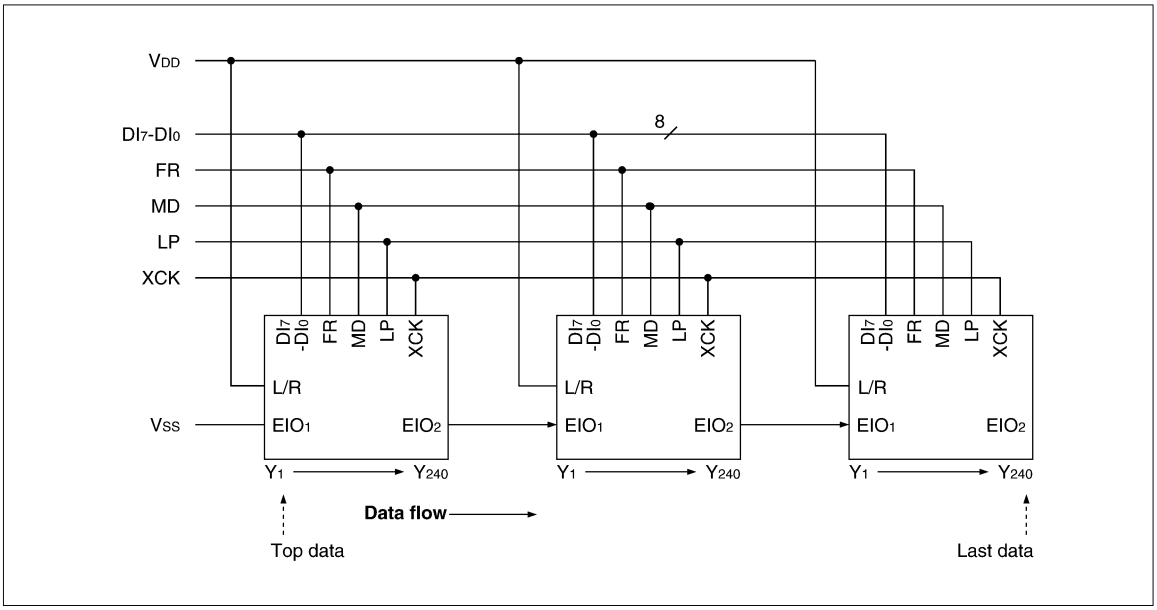
- L : V_{SS} (0 V), H : VDD (+2.5 to +5.5 V), X : Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.

CONNECTION EXAMPLES OF PLURAL SEGMENT DRIVERS

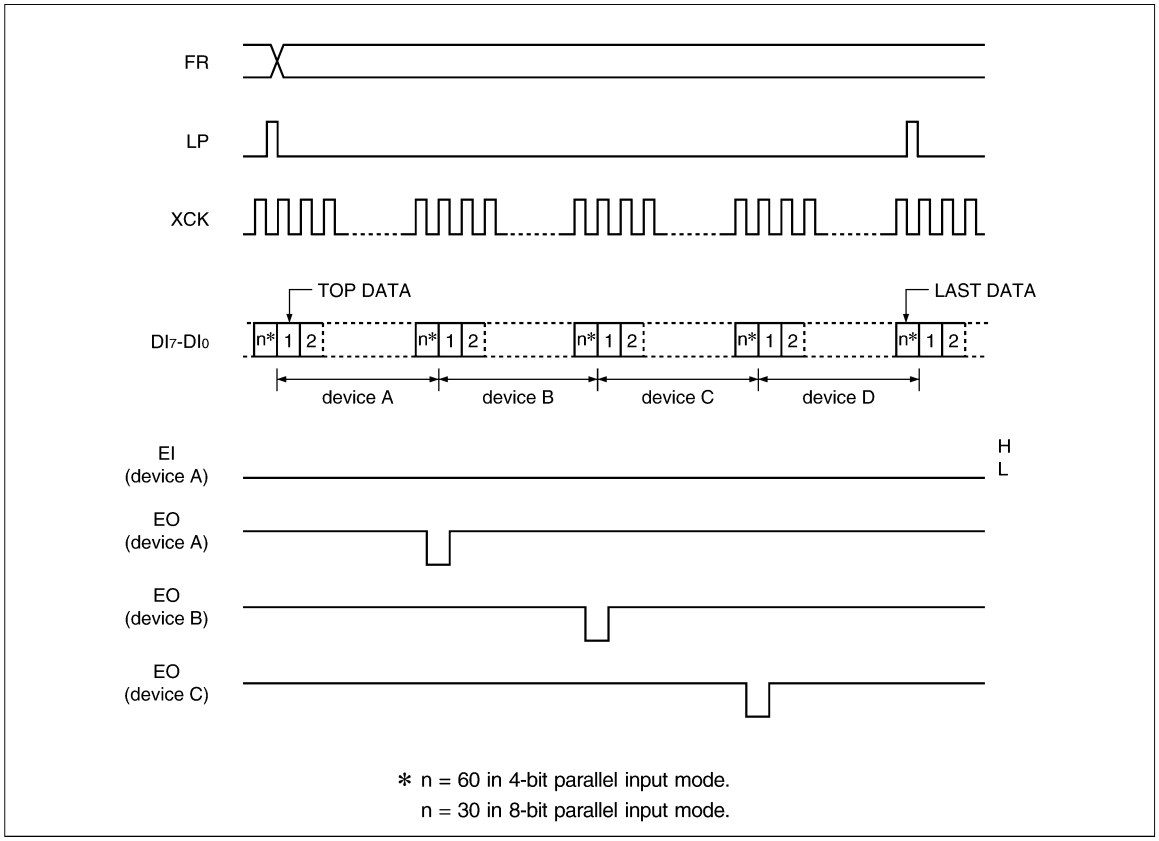
(a) When L/R = "L"



(b) When L/R = "H"



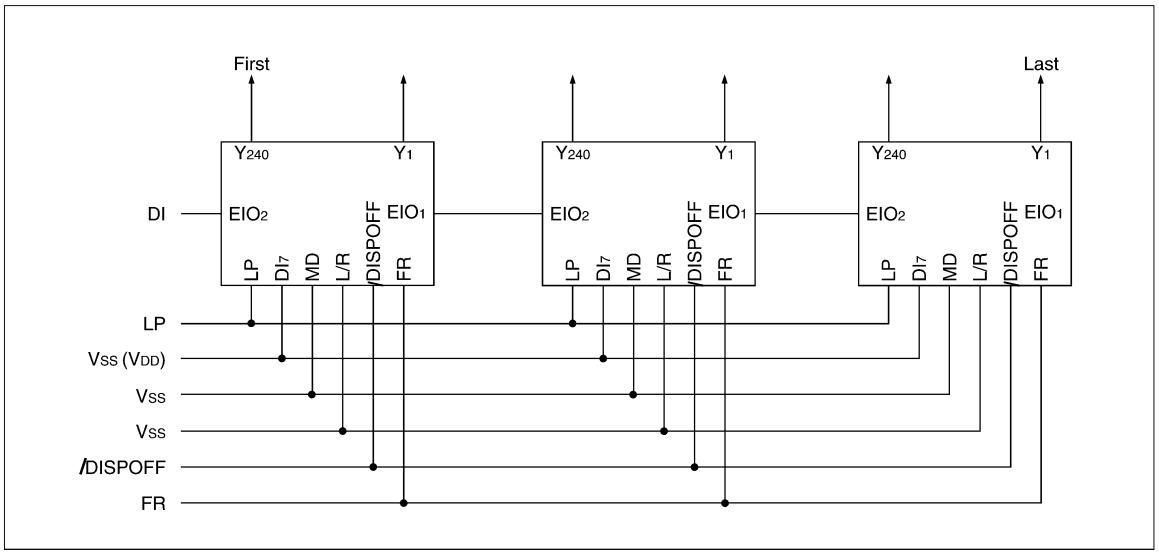
TIMING CHART OF 4-DEVICE CASCADE CONNECTION OF SEGMENT DRIVERS



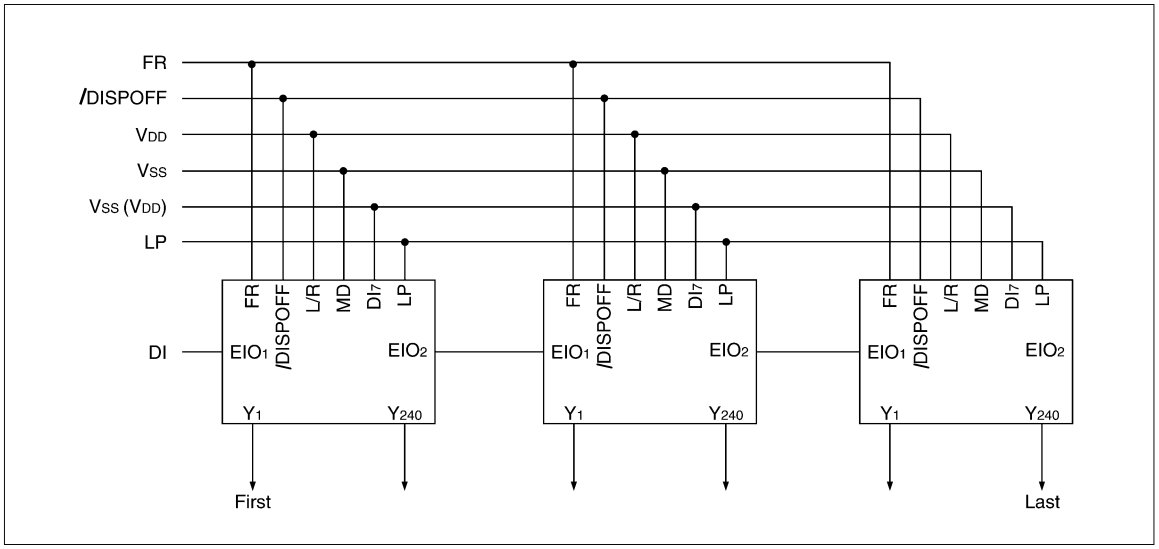
* n = 60 in 4-bit parallel input mode.
n = 30 in 8-bit parallel input mode.

CONNECTION EXAMPLES FOR PLURAL COMMON DRIVERS

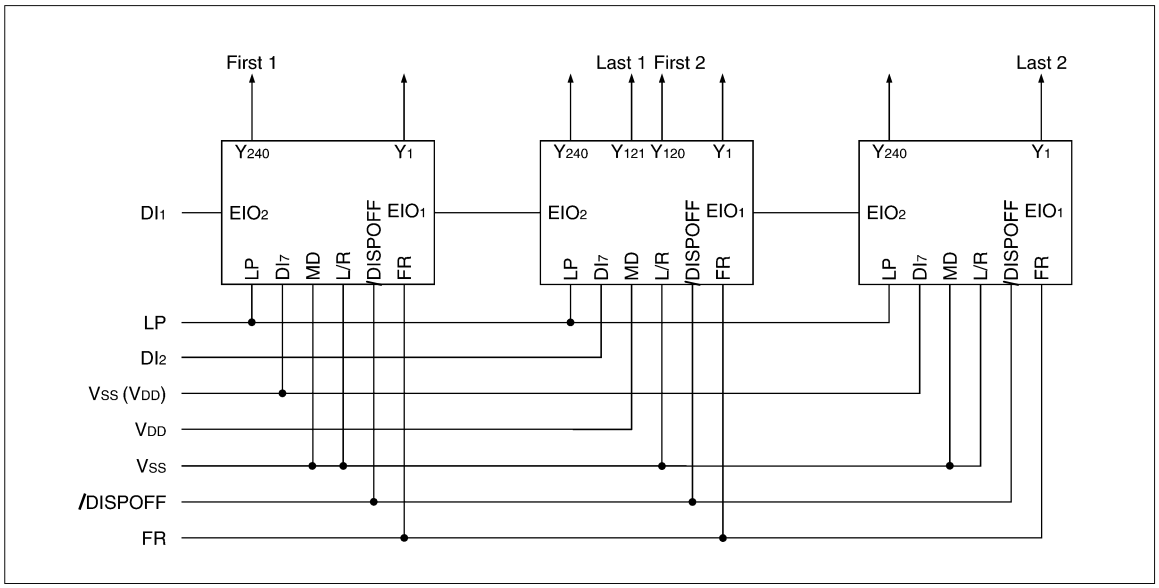
(a) Single Mode (L/R = "L")



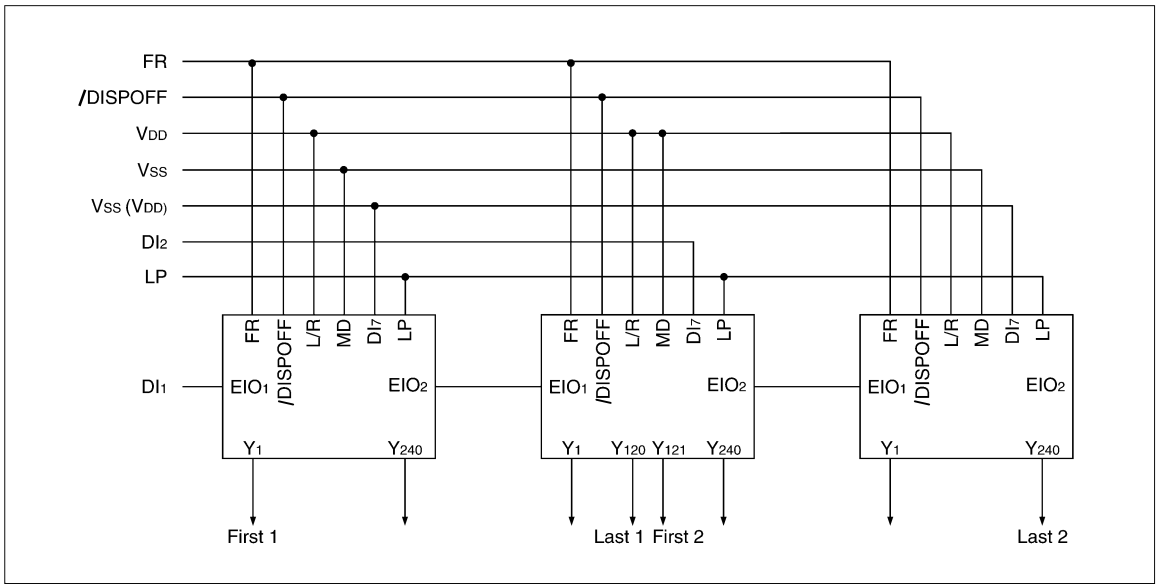
(b) Single Mode (L/R = "H")



(c) Dual Mode (L/R = "L")



(d) Dual Mode (L/R = "H")



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	-0.3 to +7.0	V	1,2
Supply voltage (2)	V_0	V_{0L}, V_{0R}	-0.3 to +40.0	V	
	V_{12}	V_{12L}, V_{12R}	-0.3 to V_0 +0.3	V	
	V_{43}	V_{43L}, V_{43R}	-0.3 to V_0 +0.3	V	
	V_5	V_{5L}, V_{5R}	-0.3 to V_0 +0.3	V	
Input voltage	V_I	DI_0-DI_7, XCL, LP, FR, MD, S/C, EIO_1, EIO_2, /DISPOFF, $TEST_1$, $TEST_2$	-0.3 to V_{DD} +0.3	V	
Storage temperature	T_{STG}		-45 to +125	℃	

NOTES :

1. TA= +25 ℃
2. The maximum applicable voltage on any pin with respect to V_{SS} (0 V).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	+2.5		+5.5	V	1,2
Supply voltage (2)	V_0	V_{0L}, V_{0R}	+15.0		+40.0	V	
Operating temperature	T_{OPR}		-30		+85	℃	

NOTES :

1. The applicable voltage on any pin with respect to V_{SS} (0 V).
2. Ensure that voltages are set such that $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Segment Mode) (V_{SS} = V_5 = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = +15.0 to +40.0 V, T_{OPR} = -30 to +85 ℃)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		DI_7-DI_0, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, /DISPOFF			0.2V_{DD}	V	
Input "High" voltage	V_{IH}			0.8V_{DD}			V	
Output "Low" voltage	V_{OL}	I_{OL}=+0.4 mA	EIO_1, EIO_2			+0.4	V	
Output "High" voltage	V_{OH}	I_{OH}=-0.4 mA		V_{DD}-0.4			V	
Input leakage current	I_{LIL}	V_I = V_{SS}	DI_7-DI_0, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, /DISPOFF			-10.0	μA	
	I_{LIH}	V_I = V_{DD}				+10.0	μA	
Output resistance	R_{ON}	|Δ V_{ON}| =0.5V, V_0=40V	Y_1-Y_{240}		1.0	1.5	KΩ	
		|Δ V_{ON}| =0.5V, V_0=30V			1.5	2.0		
		|Δ V_{ON}| =0.5V, V_0=20V			2.0	2.5		
Standby current	I_{STB}		V_{SS}			75.0	μA	1
Supply current (1) (Non-selection)	I_{DD1}		V_{DD}			2.0	mA	2
Supply current (2) (selection)	I_{DD2}		V_{DD}			12.0	mA	3
Supply current (3)	I_0		V_{0L}, V_{0R}			1.5	mA	4

NOTES :

1. V_{DD} = +5.0 V, V_0 = +40.0 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}.
2. V_{DD} = +5.0 V, V_0 = +40.0 V, f_{XCK} = 8 MHz, no-load, EI = V_{DD}.
   The input data is turned over by data taking clock (4-bit parallel input mode).
3. V_{DD} = +5.0 V, V_0 = +40.0 V, f_{XCK} = 8 MHz, no-load, EI = V_{SS}.
   The input data is turned over by data taking clock (4-bit parallel input mode).
4. V_{DD} = +5.0 V, V_0 = +40.0 V, f_{XCK} = 8 MHz, f_{LP} = 41.6 kHz, f_{FR} = 80 Hz, no-load.
   The input data is turned over by data taking clock (4-bit parallel input mode).

(Common Mode) (V_{SS}= V_5= 0 V, V_{DD}= +2.5 to +5.5 V, V_0= +15.0 to +40.0 V, T_{OPR}= -30 to +85 ℃)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		DI_7-DI_0, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, /DISPOFF			$0.2V_{DD}$	V	
Input "High" voltage	V_{IH}			$0.8V_{DD}$			V	
Output "Low" voltage	V_{OL}	I_{OL}=+0.4 mA	EIO_1, EIO_2			+0.4	V	
Output "High" voltage	V_{OH}	I_{OH}=-0.4 mA		V_{DD}-0.4			V	
Input leakage current	I_{LIL}	$V_I = V_{SS}$	DI_7-DI_0, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, /DISPOFF			-10.0	μA	
	I_{LIH}	$V_I = V_{DD}$	DI_6-DI_0, LP, L/R, FR, MD, S/C, /DISPOFF			+10.0	μA	
Input pull-down current	I_{PD}	$V_I = V_{DD}$	DI_7, XCK, EIO_1, EIO_2			100.0	μA	3
						200.0	μA	4
Output resistance	R_{ON}	$\lvert\Delta V_{ON}\rvert$ =0.5V, V_0=40V	Y_1-Y_{240}		1.0	1.5	KΩ	
		$\lvert\Delta V_{ON}\rvert$ =0.5V, V_0=30V			1.5	2.0		
		$\lvert\Delta V_{ON}\rvert$ =0.5V, V_0=20V			2.0	2.5		
Standby current	I_{STB}		V_{SS}			75.0	μA	1
Supply current (1)	I_{DD}		V_{DD}			120.0	μA	2
Supply current (2)	I_0		V_{0L}, V_{0R}			240.0	μA	2

NOTES :

1. V_{DD} = +5.0 V, V_0 = +40.0 V, V_I = V_{SS}
2. V_{DD} = +5.0 V, V_0 = +40.0 V, f_{LP} = 41.6 kHz, f_{FR} = 80 Hz, 1/480 duty operation, no-load.
3. V_{DD}= +2.5 to +3.3 V
4. V_{DD}= +3.3 to +5.5 V

AC Characteristics

(Segment Mode 1) (V_{SS} = V_5 = 0 V, V_{DD} = +5.0 ± 0.5 V, V_0 = +15.0 to +40.0 V, T_{OPR} = -30 to +85 ℃)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R, t_F ≤ 10 ns	50			ns	1
Shift clock "H" pulse width	t_{WCKH}		15			ns	
Shift clock "L" pulse width	t_{WCKL}		15			ns	
Data setup time	t_{DS}		10			ns	
Data hold time	t_{DH}		12			ns	
Latch pulse "H" pulse width	t_{WLPH}		15			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		30			ns	
Latch pulse rise to shift clock rise time	t_{LS}		25			ns	
Latch pulse fall to shift clock fall time	t_{LH}		25			ns	
Enable setup time	t_S		10			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
/DISPOFF removal time	t_{SD}		100			ns	
/DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	C_L= 15 pF			30	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	C_L= 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	C_L= 15 pF			1.2	µs	

NOTES :

1. Takes the cascade connection into consideration.
2. (t_{WCK}- t_{WCKH}- t_{WCKL})/2 is maximum in the case of high speed operation.

AC Characteristics

(Segment Mode 2) (V_{SS} = V_5 = 0 V, V_{DD} = +3.0 to +4.5 V, V_0 = +15.0 to +40.0 V, T_{OPR} = -30 to +85 ℃)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R, t_F ≤ 10 ns	66			ns	1
Shift clock "H" pulse width	t_{WCKH}		23			ns	
Shift clock "L" pulse width	t_{WCKL}		23			ns	
Data setup time	t_{DS}		15			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		50			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
/DISPOFF removal time	t_{SD}		100			ns	
/DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	C_L= 15 pF			41	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	C_L= 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	C_L= 15 pF			1.2	µs	

NOTES :

3. Takes the cascade connection into consideration.
4. (t_{WCK}- t_{WCKH}- t_{WCKL})/2 is maximum in the case of high speed operation.

AC Characteristics

(Segment Mode 3) (V_{SS} = V_5 = 0 V, V_{DD} = +2.5 to +3.0 V, V_0 = +15.0 to +40.0 V, T_{OPR} = -30 to +85 ℃)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R, t_F ≤ 10 ns	82			ns	1
Shift clock "H" pulse width	t_{WCKH}		28			ns	
Shift clock "L" pulse width	t_{WCKL}		28			ns	
Data setup time	t_{DS}		20			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		65			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
/DISPOFF removal time	t_{SD}		100			ns	
/DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	C_L= 15 pF			57	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	C_L= 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	C_L= 15 pF			1.2	µs	

NOTES :

5. Takes the cascade connection into consideration.
6. (t_{WCK}- t_{WCKH}- t_{WCKL})/2 is maximum in the case of high speed operation.

Timing Chart of Segment Mode

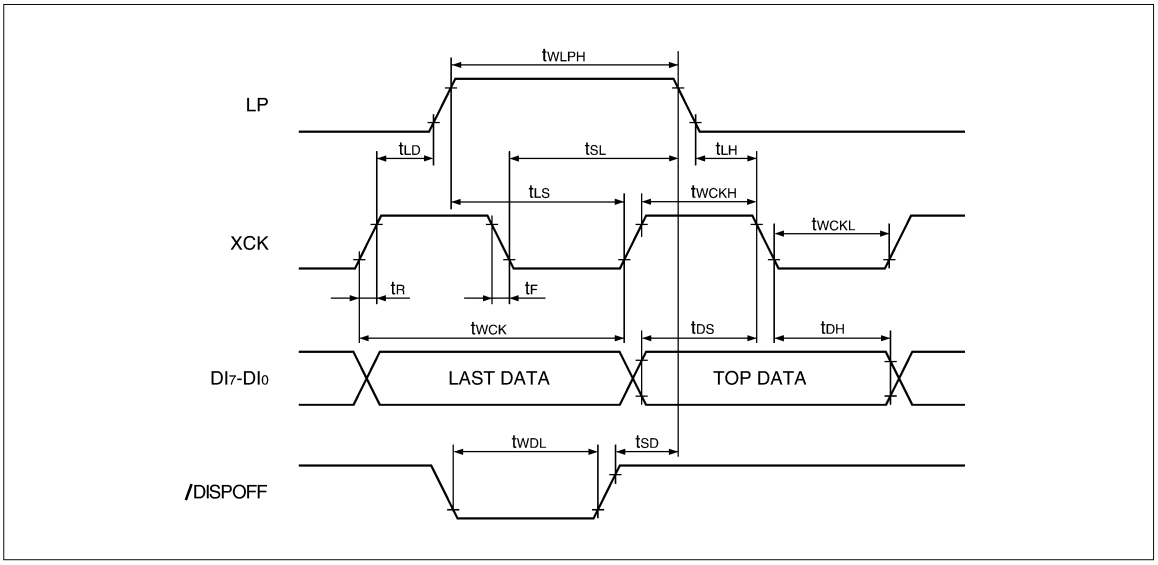
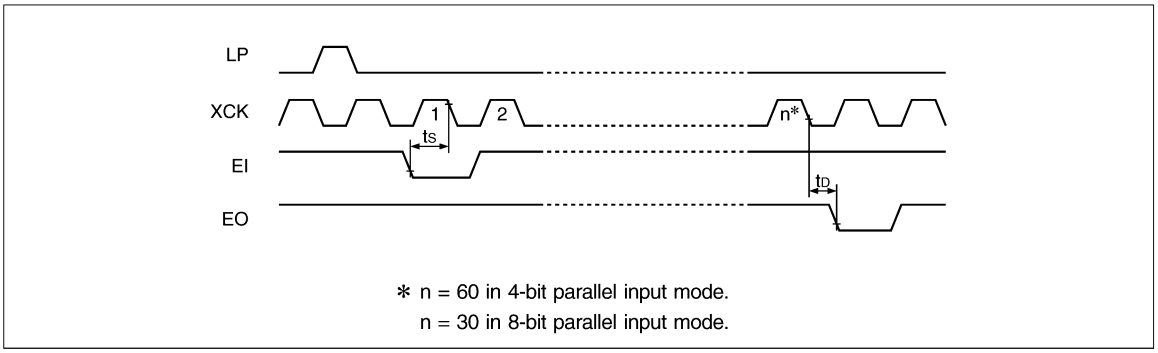


Fig. 6 Timing Characteristics (1)



* n = 60 in 4-bit parallel input mode.
n = 30 in 8-bit parallel input mode.

Fig. 7 Timing Characteristics (2)

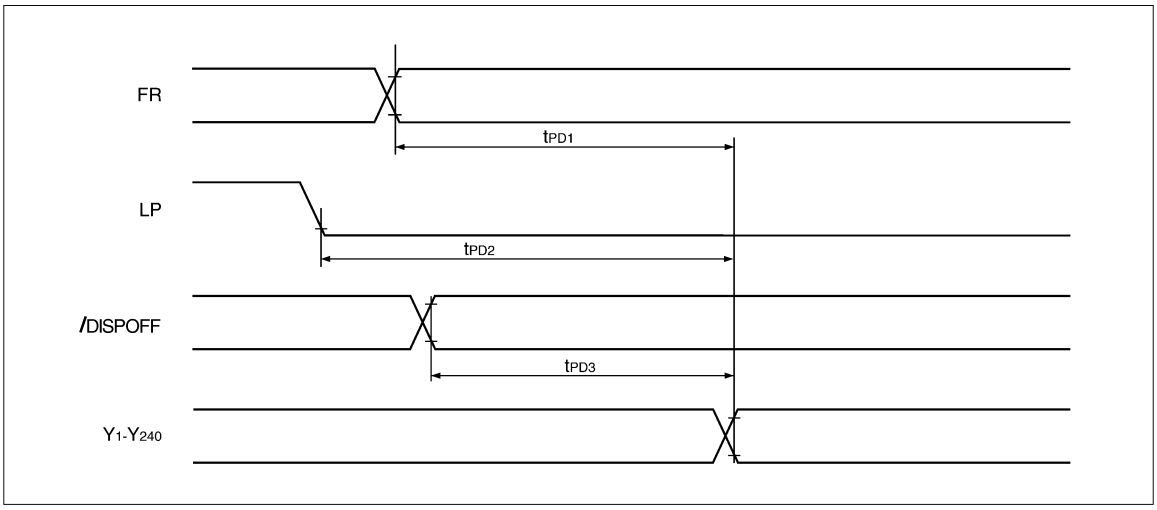
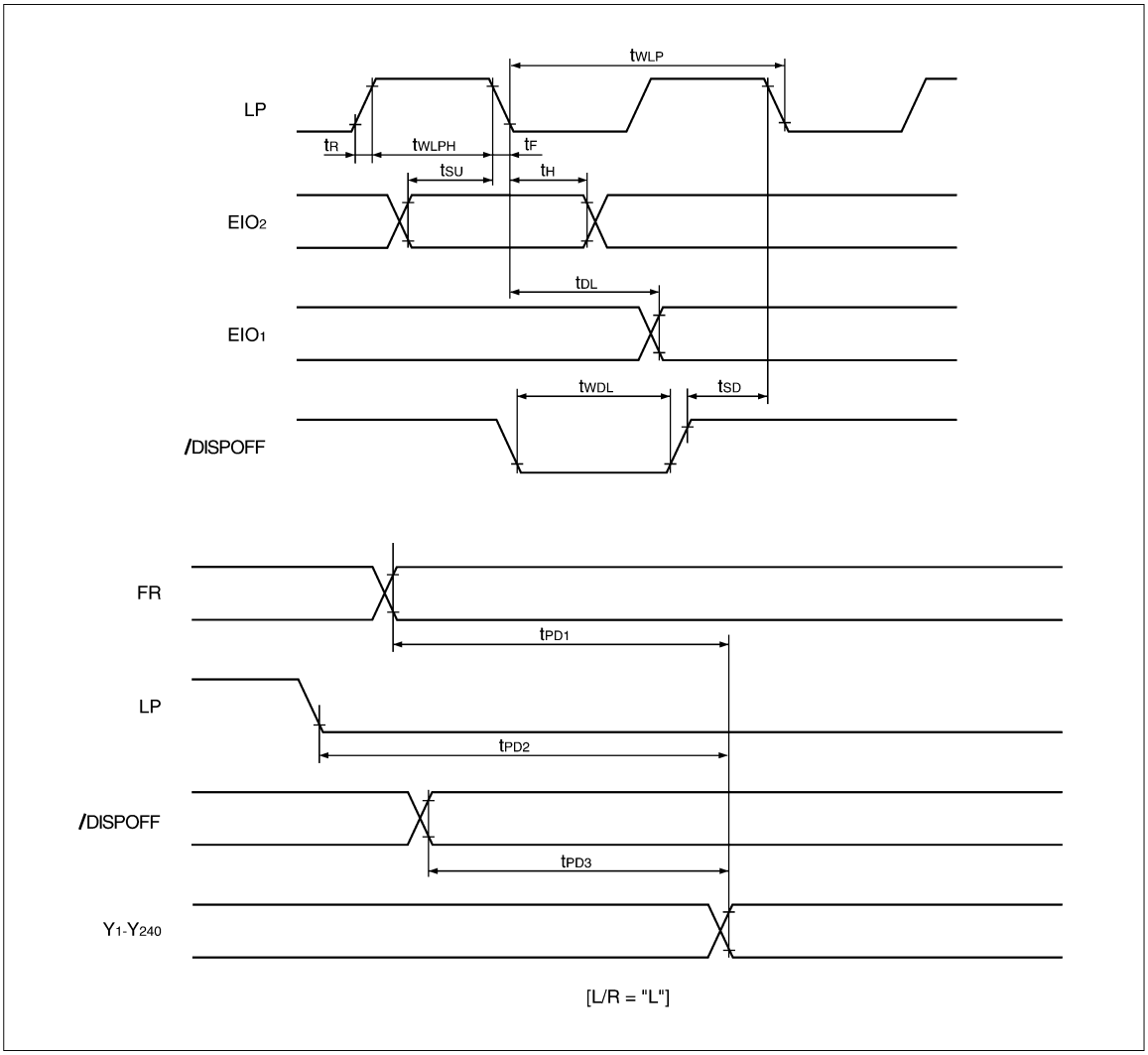


Fig. 8 Timing Characteristics (3)

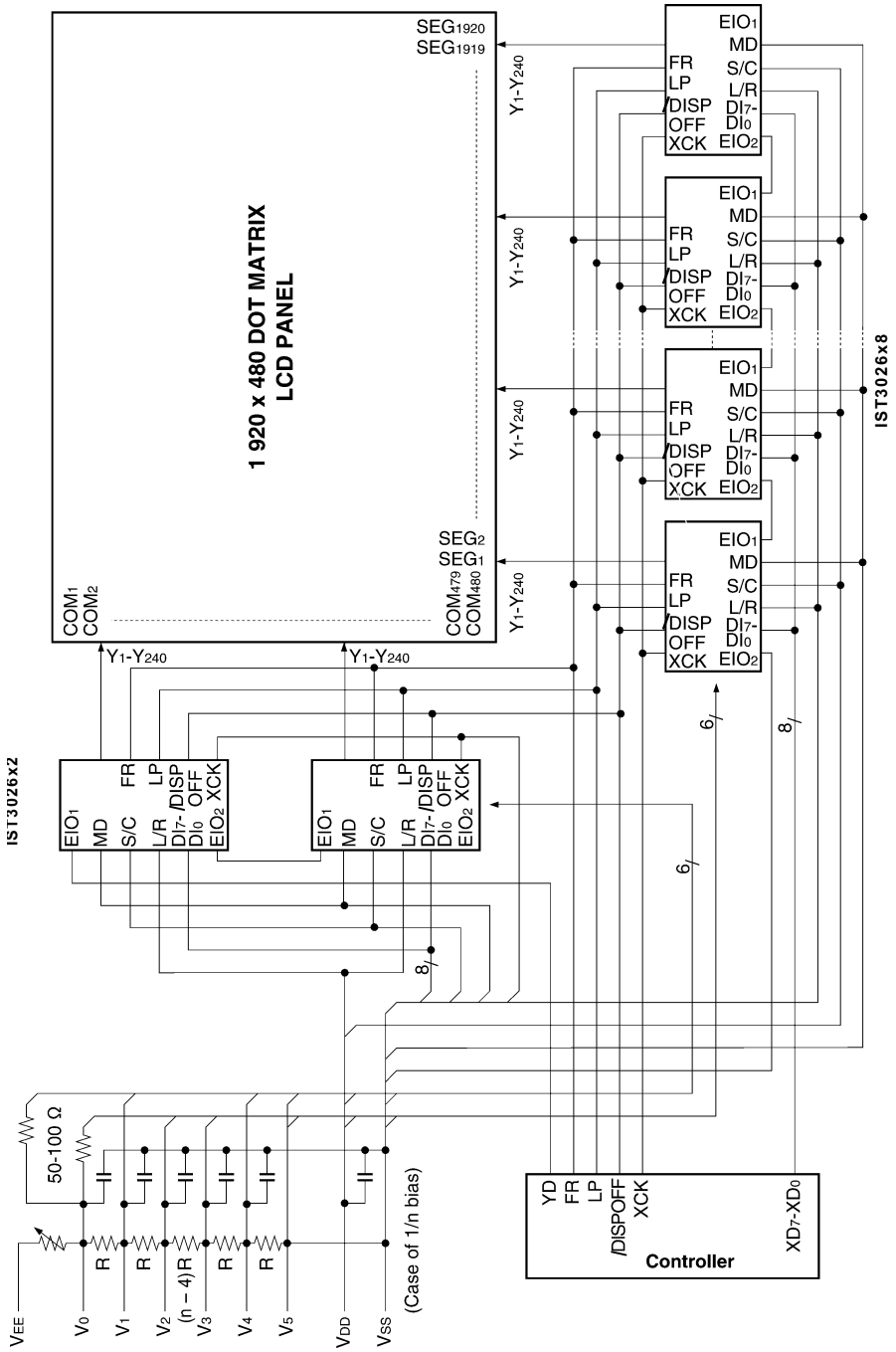
(Common Mode) (V_{SS} = V_5 = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = +15.0 to +40.0 V, T_{OPR} = -30 to +85 ℃)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Shift clock period	t_{WLP}	t_R, t_F ≤ 20 ns	250			ns
Shift clock "H" pulse width	t_{WLPH}	V_{DD} = +5.0 ± 0.5V	15			ns
		V_{DD} = +2.5 to + 4.5V	30			ns
Data setup time	t_{SU}		30			ns
Data hold time	t_H		50			ns
Input signal rise time	t_R				50	ns
Input signal fall time	t_F				50	ns
/DISPOFF removal time	t_{SD}		100			ns
/DISPOFF "L" pulse width	T_{WDL}		1.2			µs
Output delay time (1)	t_{DL}	C_L= 15 pF			200	ns
Output delay time (2)	t_{PD1}, t_{PD2}	C_L= 15 pF			1.2	µs
Output delay time (3)	t_{PD3}	C_L= 15 pF			1.2	µs

Timing Chart of Common Mode



SYSTEM CONFIGURATION EXAMPLE



PRECAUTIONS

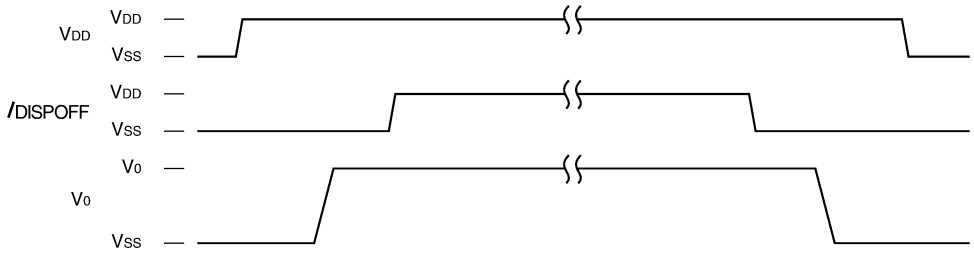
Precautions when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. The details are as follows.

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power.
- It is advisable to connect the serial resistor (50 to 100 Ω) or fuse to the LCD drive power V_0 of the system as a current limiter. Set up a suitable value of the resistor in consideration of the display grade.

And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on /DISPOFF function. After that, cancel the /DISPOFF function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level V_5 on /DISPOFF function. Then, disconnect the logic system power after disconnecting the LCD drive power.

When connecting the power supply, follow the recommended sequence shown here.



PAD CONFIGURATION :

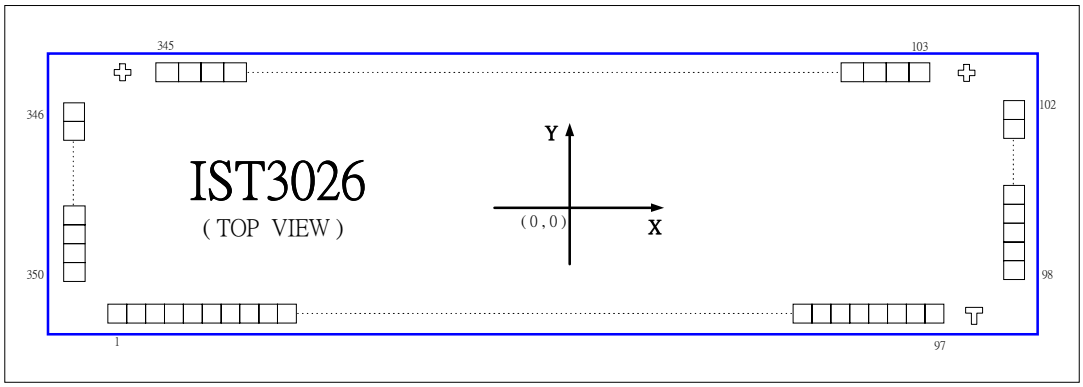
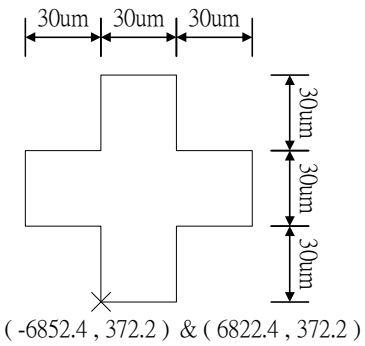


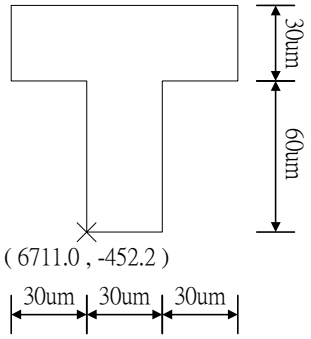
Figure 1 : IST3026 Chip Configuration

Table 1. IST3026 Pad Dimensions ※Note: All dummy pads have gold bumps.

Item	Pad No.	Size		Unit
		X	Y	
Chip size	350	13940	1080	um
Pad pitch	1 to 102, 346 to 350	100 (min)		
	103 to 345	55 (min)		
Bumped pad size	1 to 8, 11 to 18, 78 to 80, 82 to 85, 91 to 97,	61	85	
	103,345	61	83	
	9 to 10, 19 to 31, 72 to 77, 81, 86 to 90,	37	85	
	104 to 344	37	83	
	32 to 71	79	37	
	98 to 102, 346 to 350	85	61	
Bumped pad height	All pad	18		

COG Align Key Coordinate





PAD CENTER COORDINATES :

Table 2 : Pad Center Coordinates

Unit : um

PAD NO	PAD NAME	COORDINATES X	COORDINATES Y	PAD NO	PAD NAME	COORDINATES X	COORDINATES Y
1	DUMMY	-6615.6	-406.2	36	DUMMY	-943.3	-426.2
2	V5	-6448.5	-406.2	37	DUMMY	-843.3	-426.2
3	VSS	-6277.9	-406.2	38	DUMMY	-743.3	-426.2
4	VSS	-6106.1	-406.2	39	DUMMY	-643.3	-426.2
5	VSS	-5934.3	-406.2	40	DUMMY	-543.3	-426.2
6	VSS	-5762.5	-406.2	41	DUMMY	-443.3	-426.2
7	VSS	-5590.7	-406.2	42	DUMMY	-343.3	-426.2
8	VSS	-5418.9	-406.2	43	DUMMY	-243.3	-426.2
9	DUMMY	-5205.4	-406.2	44	DUMMY	-143.3	-426.2
10	DUMMY	-5145.4	-406.2	45	DUMMY	-43.3	-426.2
11	VSS	-4988.3	-406.2	46	DUMMY	56.7	-426.2
12	VSS	-4821.0	-406.2	47	DUMMY	156.7	-426.2
13	VSS	-4653.7	-406.2	48	DUMMY	256.7	-426.2
14	VSS	-4486.4	-406.2	49	DUMMY	356.7	-426.2
15	VSS	-4319.1	-406.2	50	DUMMY	456.7	-426.2
16	VDD	-4145.0	-406.2	51	DUMMY	556.7	-426.2
17	VDD	-3970.9	-406.2	52	DUMMY	656.7	-426.2
18	VDD	-3796.8	-406.2	53	DUMMY	756.7	-426.2
19	SC	-3656.1	-406.2	54	DUMMY	856.7	-426.2
20	VSS	-3460.4	-406.2	55	DUMMY	956.7	-426.2
21	EIO2	-3314.4	-406.2	56	DUMMY	1056.7	-426.2
22	DI0	-3118.7	-406.2	57	DUMMY	1156.7	-426.2
23	DI1	-2946.3	-406.2	58	DUMMY	1256.7	-426.2
24	DI2	-2750.1	-406.2	59	DUMMY	1356.7	-426.2
25	DI3	-2577.7	-406.2	60	DUMMY	1456.7	-426.2
26	VSS	-2382.0	-406.2	61	DUMMY	1556.7	-426.2
27	DI4	-2241.5	-406.2	62	DUMMY	1656.7	-426.2
28	DI5	-2045.3	-406.2	63	DUMMY	1756.7	-426.2
29	DI6	-1872.9	-406.2	64	DUMMY	1856.7	-426.2
30	DI7	-1676.7	-406.2	65	DUMMY	1956.7	-426.2
31	XCK	-1504.3	-406.2	66	DUMMY	2056.7	-426.2
32	DUMMY	-1343.3	-426.2	67	DUMMY	2156.7	-426.2
33	DUMMY	-1243.3	-426.2	68	DUMMY	2256.7	-426.2
34	DUMMY	-1143.3	-426.2	69	DUMMY	2356.7	-426.2
35	DUMMY	-1043.3	-426.2	70	DUMMY	2456.7	-426.2

Table 2 : Pad Center Coordinates (Continued)

Unit : um

PAD NO	PAD NAME	COORDINATES X	COORDINATES Y	PAD NO	PAD NAME	COORDINATES X	COORDINATES Y
71	DUMMY	2556.7	-426.2	106	Y3	6517.5	420.0
72	/DISPOFF	2707.0	-406.2	107	Y4	6462.5	420.0
73	LP	2903.2	-406.2	108	Y5	6407.5	420.0
74	EIO1	3075.6	-406.2	109	Y6	6352.5	420.0
75	FR	3271.3	-406.2	110	Y7	6297.5	420.0
76	VSS	3407.5	-406.2	111	Y8	6242.5	420.0
77	L/R	3603.2	-406.2	112	Y9	6187.5	420.0
78	VDD	3743.9	-406.2	113	Y10	6132.5	420.0
79	VDD	3918.0	-406.2	114	Y11	6077.5	420.0
80	VDD	4092.1	-406.2	115	Y12	6022.5	420.0
81	MD	4309.8	-406.2	116	Y13	5967.5	420.0
82	VSS	4455.5	-406.2	117	Y14	5912.5	420.0
83	VSS	4624.6	-406.2	118	Y15	5857.5	420.0
84	VSS	4793.7	-406.2	119	Y16	5802.5	420.0
85	VSS	4962.8	-406.2	120	Y17	5747.5	420.0
86	DUMMY	5119.9	-406.2	121	Y18	5692.5	420.0
87	DUMMY	5179.9	-406.2	122	Y19	5637.5	420.0
88	DUMMY	5239.9	-406.2	123	Y20	5582.5	420.0
89	DUMMY	5299.9	-406.2	124	Y21	5527.5	420.0
90	DUMMY	5359.9	-406.2	125	Y22	5472.5	420.0
91	VSS	5595.6	-406.2	126	Y23	5417.5	420.0
92	VSS	5767.4	-406.2	127	Y24	5362.5	420.0
93	VSS	5939.2	-406.2	128	Y25	5307.5	420.0
94	VSS	6111.0	-406.2	129	Y26	5252.5	420.0
95	VSS	6282.8	-406.2	130	Y27	5197.5	420.0
96	V5	6446.9	-406.2	131	Y28	5142.5	420.0
97	DUMMY	6615.6	-406.2	132	Y29	5087.5	420.0
98	DUMMY	6840.0	-338.4	133	Y30	5032.5	420.0
99	V43	6840.0	-180.4	134	Y31	4977.5	420.0
100	V12	6840.0	24.0	135	Y32	4922.5	420.0
101	V0	6840.0	241.2	136	Y33	4867.5	420.0
102	DUMMY	6840.0	325.2	137	Y34	4812.5	420.0
103	DUMMY	6699.5	420.0	138	Y35	4757.5	420.0
104	Y1	6627.5	420.0	139	Y36	4702.5	420.0
105	Y2	6572.5	420.0	140	Y37	4647.5	420.0

Table 2 : Pad Center Coordinates (Continued)

Unit : um

PAD NO	PAD NAME	COORDINATES X	COORDINATES Y	PAD NO	PAD NAME	COORDINATES X	COORDINATES Y
141	Y38	4592.5	420.0	176	Y73	2667.5	420.0
142	Y39	4537.5	420.0	177	Y74	2612.5	420.0
143	Y40	4482.5	420.0	178	Y75	2557.5	420.0
144	Y41	4427.5	420.0	179	Y76	2502.5	420.0
145	Y42	4372.5	420.0	180	Y77	2447.5	420.0
146	Y43	4317.5	420.0	181	Y78	2392.5	420.0
147	Y44	4262.5	420.0	182	Y79	2337.5	420.0
148	Y45	4207.5	420.0	183	Y80	2282.5	420.0
149	Y46	4152.5	420.0	184	Y81	2227.5	420.0
150	Y47	4097.5	420.0	185	Y82	2172.5	420.0
151	Y48	4042.5	420.0	186	Y83	2117.5	420.0
152	Y49	3987.5	420.0	187	Y84	2062.5	420.0
153	Y50	3932.5	420.0	188	Y85	2007.5	420.0
154	Y51	3877.5	420.0	189	Y86	1952.5	420.0
155	Y52	3822.5	420.0	190	Y87	1897.5	420.0
156	Y53	3767.5	420.0	191	Y88	1842.5	420.0
157	Y54	3712.5	420.0	192	Y89	1787.5	420.0
158	Y55	3657.5	420.0	193	Y90	1732.5	420.0
159	Y56	3602.5	420.0	194	Y91	1677.5	420.0
160	Y57	3547.5	420.0	195	Y92	1622.5	420.0
161	Y58	3492.5	420.0	196	Y93	1567.5	420.0
162	Y59	3437.5	420.0	197	Y94	1512.5	420.0
163	Y60	3382.5	420.0	198	Y95	1457.5	420.0
164	Y61	3327.5	420.0	199	Y96	1402.5	420.0
165	Y62	3272.5	420.0	200	Y97	1347.5	420.0
166	Y63	3217.5	420.0	201	Y98	1292.5	420.0
167	Y64	3162.5	420.0	202	Y99	1237.5	420.0
168	Y65	3107.5	420.0	203	Y100	1182.5	420.0
169	Y66	3052.5	420.0	204	Y101	1127.5	420.0
170	Y67	2997.5	420.0	205	Y102	1072.5	420.0
171	Y68	2942.5	420.0	206	Y103	1017.5	420.0
172	Y69	2887.5	420.0	207	Y104	962.5	420.0
173	Y70	2832.5	420.0	208	Y105	907.5	420.0
174	Y71	2777.5	420.0	209	Y106	852.5	420.0
175	Y72	2722.5	420.0	210	Y107	797.5	420.0

Table 2 : Pad Center Coordinates (Continued)

Unit : um

PAD NO	PAD NAME	COORDINATES X	COORDINATES Y	PAD NO	PAD NAME	COORDINATES X	COORDINATES Y
211	Y108	742.5	420.0	246	Y142	-1237.5	420.0
212	Y109	687.5	420.0	247	Y143	-1292.5	420.0
213	Y110	632.5	420.0	248	Y144	-1347.5	420.0
214	Y111	577.5	420.0	249	Y145	-1402.5	420.0
215	Y112	522.5	420.0	250	Y146	-1457.5	420.0
216	Y113	467.5	420.0	251	Y147	-1512.5	420.0
217	Y114	412.5	420.0	252	Y148	-1567.5	420.0
218	Y115	357.5	420.0	253	Y149	-1622.5	420.0
219	Y116	302.5	420.0	254	Y150	-1677.5	420.0
220	Y117	247.5	420.0	255	Y151	-1732.5	420.0
221	Y118	192.5	420.0	256	Y152	-1787.5	420.0
222	Y119	137.5	420.0	257	Y153	-1842.5	420.0
223	Y120	82.5	420.0	258	Y154	-1897.5	420.0
224	DUMMY	0.0	420.0	259	Y155	-1952.5	420.0
225	Y121	-82.5	420.0	260	Y156	-2007.5	420.0
226	Y122	-137.5	420.0	261	Y157	-2062.5	420.0
227	Y123	-192.5	420.0	262	Y158	-2117.5	420.0
228	Y124	-247.5	420.0	263	Y159	-2172.5	420.0
229	Y125	-302.5	420.0	264	Y160	-2227.5	420.0
230	Y126	-357.5	420.0	265	Y161	-2282.5	420.0
231	Y127	-412.5	420.0	266	Y162	-2337.5	420.0
232	Y128	-467.5	420.0	267	Y163	-2392.5	420.0
233	Y129	-522.5	420.0	268	Y164	-2447.5	420.0
234	Y130	-577.5	420.0	269	Y165	-2502.5	420.0
235	Y131	-632.5	420.0	270	Y166	-2557.5	420.0
236	Y132	-687.5	420.0	271	Y167	-2612.5	420.0
237	Y133	-742.5	420.0	272	Y168	-2667.5	420.0
238	Y134	-797.5	420.0	273	Y169	-2722.5	420.0
239	Y135	-852.5	420.0	274	Y170	-2777.5	420.0
240	Y136	-907.5	420.0	275	Y171	-2832.5	420.0
241	Y137	-962.5	420.0	276	Y172	-2887.5	420.0
242	Y138	-1017.5	420.0	277	Y173	-2942.5	420.0
243	Y139	-1072.5	420.0	278	Y174	-2997.5	420.0
244	Y140	-1127.5	420.0	279	Y175	-3052.5	420.0
245	Y141	-1182.5	420.0	280	Y176	-3107.5	420.0

Table 2 : Pad Center Coordinates (Continued)

Unit : um

PAD NO	PAD NAME	COORDINATES X	COORDINATES Y	PAD NO	PAD NAME	COORDINATES X	COORDINATES Y
281	Y177	-3162.5	420.0	316	Y212	-5087.5	420.0
282	Y178	-3217.5	420.0	317	Y213	-5142.5	420.0
283	Y179	-3272.5	420.0	318	Y214	-5197.5	420.0
284	Y180	-3327.5	420.0	319	Y215	-5252.5	420.0
285	Y181	-3382.5	420.0	320	Y216	-5307.5	420.0
286	Y182	-3437.5	420.0	321	Y217	-5362.5	420.0
287	Y183	-3492.5	420.0	322	Y218	-5417.5	420.0
288	Y184	-3547.5	420.0	323	Y219	-5472.5	420.0
289	Y185	-3602.5	420.0	324	Y220	-5527.5	420.0
290	Y186	-3657.5	420.0	325	Y221	-5582.5	420.0
291	Y187	-3712.5	420.0	326	Y222	-5637.5	420.0
292	Y188	-3767.5	420.0	327	Y223	-5692.5	420.0
293	Y189	-3822.5	420.0	328	Y224	-5747.5	420.0
294	Y190	-3877.5	420.0	329	Y225	-5802.5	420.0
295	Y191	-3932.5	420.0	330	Y226	-5857.5	420.0
296	Y192	-3987.5	420.0	331	Y227	-5912.5	420.0
297	Y193	-4042.5	420.0	332	Y228	-5967.5	420.0
298	Y194	-4097.5	420.0	333	Y229	-6022.5	420.0
299	Y195	-4152.5	420.0	334	Y230	-6077.5	420.0
300	Y196	-4207.5	420.0	335	Y231	-6132.5	420.0
301	Y197	-4262.5	420.0	336	Y232	-6187.5	420.0
302	Y198	-4317.5	420.0	337	Y233	-6242.5	420.0
303	Y199	-4372.5	420.0	338	Y234	-6297.5	420.0
304	Y200	-4427.5	420.0	339	Y235	-6352.5	420.0
305	Y201	-4482.5	420.0	340	Y236	-6407.5	420.0
306	Y202	-4537.5	420.0	341	Y237	-6462.5	420.0
307	Y203	-4592.5	420.0	342	Y238	-6517.5	420.0
308	Y204	-4647.5	420.0	343	Y239	-6572.5	420.0
309	Y205	-4702.5	420.0	344	Y240	-6627.5	420.0
310	Y206	-4757.5	420.0	345	DUMMY	-6699.5	420.0
311	Y207	-4812.5	420.0	346	DUMMY	-6840.0	325.2
312	Y208	-4867.5	420.0	347	V0	-6840.0	241.2
313	Y209	-4922.5	420.0	348	V12	-6840.0	24.0
314	Y210	-4977.5	420.0	349	V43	-6840.0	-180.4
315	Y211	-5032.5	420.0	350	DUMMY	-6840.0	-338.4