PHOENIX DISPLAY
INTERNATIONAL, INC.

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SPECIFICATION FOR LCD MODULE

CUSTOMER	
PART NUMBER	PDIAT23901
DESCRIPTION	1.46" 128 x 3 x 128 Dots
VERSION	
ISSUE DATE	

COMPANY ADDRESS:
Phoenix Display International, Inc.
6150 W. Gila Springs Place Unit 2
Chandler, AZ 85226
USA
www.phoenixdisplay.com
(630) 359-5700 office
(630) 359-5701 fax

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	INITIAL RELEASE	2009. 03. 16	
X02	■ Modify luminance specifications ■ Add the panel electrical specifications	2009. 07. 02	Page 6, 7 & 8
A01	■ Transfer from X version ■ Add the information of module weight ■ Add the packing specification	2009. 07. 24	Page 5 & 17

CONTENTS

1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by A-TOPS This document, together with the Module Drawing, is the highest level specification for this product. It describes the product, identifies supporting documents and contains specifications.

2.FEATURES

- Small molecular organic light emitting diode.
- Color : 262K color and 65K colors
- Panel matrix : 128*128
- Driver IC : SSD1351
- Excellent quick response time.
- Extremely thin thickness for best mechanism design : 1.61mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- Strong environmental resistance.
- 8/16/18-bit 6800-series Parallel Interface, 8/16/18-bit 8080-series Parallel Interface, Serial Peripheral Interface.
- Wide range of operating temperature : -40 to 70 °C.
- Anti-glare polarizer.

3.MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 (W) x (RxGxB) x 128 (H)	dot
2	Dot Size	0.0435 (W) x 0.1855 (H)	mm^2
3	Dot Pitch	0.0685 (W) x 0.2055 (H)	mm^2
4	Aperture Rate	57	%
5	Active Area	26.279 (W) x 26.284 (H)	mm^2
6	Panel Size	33.5 (W) x 33.5 (H)	mm^2
7*	Panel Thickness	1.42 ± 0.1	mm
8	Module Size	33.5 (W) x 46.33 (H) x 1.61 (D)	mm^3
9	Diagonal A/A size	1.46	inch
10	Module Weight	3.93 ± 10%	gram

* Panel thickness includes substrate glass, cover glass and UV glue thickness.

4.MA XIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{CI})	-0.3	4	V	Ta = 25°C	IC maximum rating
Supply Voltage (Vcc)	10	19	V	Ta = 25°C	IC maximum rating
Supply Voltage (V_{DDIO})	-0.5	V_{CI}	V	Ta = 25°C	IC maximum rating
Operating Temp.	-40	70	°C		
Storage Temp	-40	85	°C		
Humidity	-	85	%		
Life Time	11,000	-	Hrs	90 cd/m^2, 50% checkerboard	Note (1)
Life Time	14,000	-	Hrs	70 cd/m^2, 50% checkerboard	Note (2)

Note:

(A) Under Vcc = 16.5V, Ta = 25°C, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 90 cd/m^2 :

- Master contrast setting : 0x0B
- Red contrast setting : 0x70
- Green contrast setting : 0x71
- Blue contrast setting : 0x94
- Frame rate : 105Hz
- Duty setting : 1/128

(2) Setting of 70 cd/m^2 :

- Master contrast setting : 0x09
- Red contrast setting : 0x66
- Green contrast setting : 0x6A
- Blue contrast setting : 0x89
- Frame rate : 105Hz
- Duty setting : 1/128

5. ELECTRICAL CHARACTERISTICS

5.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Analog power supply (for OLED panel)		16	16.5	17	V
V_{CI}	Digital power supply		2.4	2.8	3.5	V
V_{DDIO}	I/O voltage power supply		1.65	-	V_{CI}	V
I_{DD}	V_{CI} = V_{DDIO} =3.5V, V_{CC} = 16V, External V_{DD} = 2.6V, Display ON, No panel attached, contrast = FF			170	190	uA
I_{DDIO}	V_{CI} = V_{DDIO} =, 3.5V, V_{CC} = 16V, Display ON, No panel attached, contrast = FF	External VDD = 2.6V		0.5	10	uA
		Internal VDD		0.5	10	uA
I_{CI}	V_{CI} = V_{DDIO} =, 3.5V, V_{CC} = 16V, Display ON, No panel attached, contrast = FF	External VDD = 2.6V	-	60	70	uA
		Internal VDD		255	280	uA
I_{CC}	V_{CI} = V_{DDIO} =, 3.5V, V_{CC} = 16V, Display ON, No panel attached, contrast = FF	External VDD = 2.6V	-	1.15	1.26	mA
		Internal VDD		1.15	1.26	mA
V_{IH}	Hi logic input level		0.8* V_{DDIO}	-	V_{DDIO}	V
V_{IL}	Low logic input level		0	-	0.2* V_{DDIO}	V
V_{OH}	Hi logic output level		0.9* V_{DDIO}	-	V_{DDIO}	V
V_{OL}	Low logic output level		0	-	0.1* V_{DDIO}	V
I_{SEG}	Segment Output Current Setting V_{CC} = 16V at IREF = 12.5uA	Contrast=FF	-	200	-	uA
		Contrast=7F	-	100	-	uA
		Contrast=3F	-	50	-	uA

5.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current		30	32	mA	All pixels on (1)
Standby mode current		3	4	mA	Standby mode 10% pixels on (2)
Normal mode power consumption		495	528	mW	All pixels on (1)
Standby mode power consumption		49.5	66	mW	Standby mode 10% pixels on (2)
Normal mode Luminance	70	90		cd/m^2	Display Average
Standby mode Luminance		20		cd/m^2	
CIEx (White)	0.24	0.28	0.32		x, y (CIE 1931)
CIEy (White)	0.28	0.32	0.36		
CIEx (Red)	0.62	0.66	0.70		
CIEy (Red)	0.29	0.33	0.37		
CIEx (Green)	0.26	0.30	0.34		
CIEy (Green)	0.59	0.63	0.67		
CIEx (Blue)	0.10	0.14	0.18		
CIEy (Blue)	0.14	0.18	0.22		
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition :

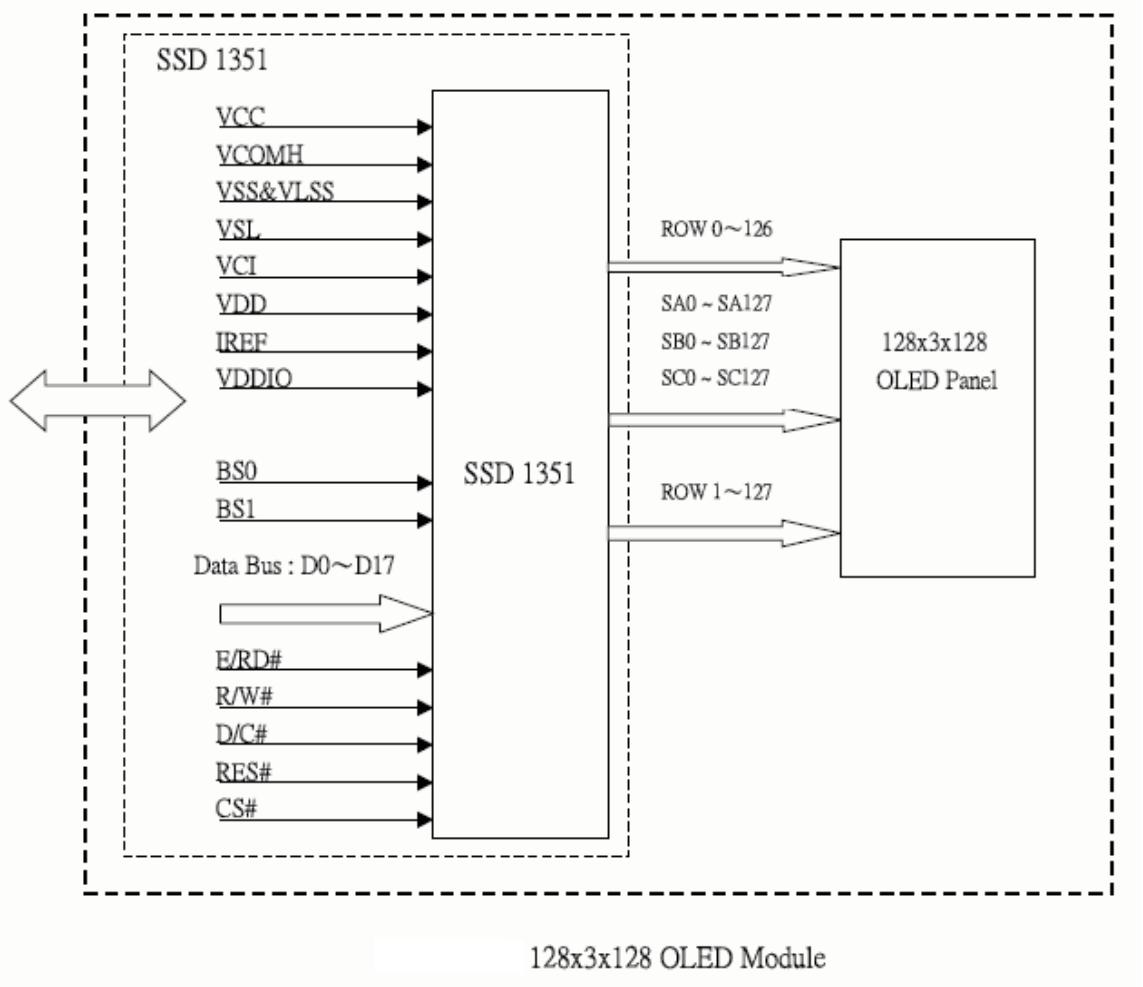
- Driving Voltage : 16.5V
- Master contrast setting : 0x0B
- Red contrast setting : 0x70
- Green contrast setting : 0x71
- Blue contrast setting : 0x94
- Frame rate : 105Hz
- Duty setting : 1/128

(2) Standby mode condition :

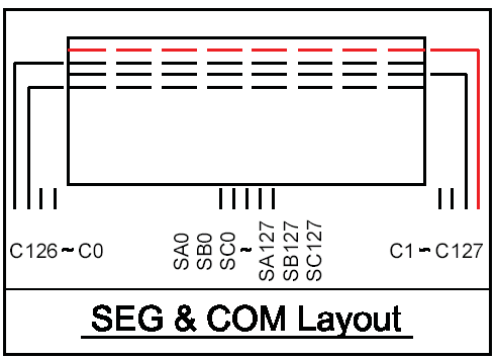
- Driving Voltage : 16.5V
- Master contrast setting : 0x04
- Red contrast setting : 0x4E
- Green contrast setting : 0x53
- Blue contrast setting : 0X6E
- Frame rate : 105Hz
- Duty setting : 1/128

6.INTERFACE

6.1 FUNCTION BLOCK DIAGRAM



6.2PANELLAYOUTDIA GRAM



6.3 PIN ASSIGNMENTS

PIN NAME	PIN NO	DESCRIPTION
NC	1	No connection.
VLSS	2	Analog system ground pin
VCC	3	Power supply for panel driving voltage.
VCI	4	Digital voltage power supply.
VDD	5	Power supply pin for core logic operation.
IREF	6	A resistor should be connected between this pin and VSS.
RES#	7	Hardware Reset pin (Low active).
D/C#	8	H: Data, L: Command.
CS#	9	Chip select pin.
BS1	10	Interface select pin.
BS0	11	Interface select pin.
R/W#	12	8080: data write enable pin; 6800:Read/Write select pin.
E/RD#	13	8080: data read enable pin; 6800:Read/Write enable pin.
D0	14	These pins are bi-directional data bus connecting to the MCU data bus.
D1	15	
D2	16	
D3	17	
D4	18	
D5	19	
D6	20	
D7	21	
D8	22	
D9	23	
D10	24	
D11	25	
D12	26	
D13	27	
D14	28	
D15	29	
D16	30	
D17	31	
VSL	32	This is segment voltage reference pin.
VDDIO	33	Power supply for interface logic level.
VCOMH	34	COM signal deselected voltage level. A capacitor should be connected between this pin an VSS.
VCC	35	Power supply for panel driving voltage.
VSS	36	Ground.
NC	37	No connection.

6.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the pattern to be displayed. The RAM size is 128 x 128 x 18bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. Each pixel has 18-bit data. Each sub-pixels for color A, B and C have 6 bits. The arrangement of data pixel in graphic display data RAM is shown below.

262k Color Depth Graphic Display Data RAM Structure

Segment Address	Normal	0			1			2	.....	.....	126	127		
	Remapped	127			126			125	.....	.....	1	0		
Color		A	B	C	A	B	C	A			C	A	B	C
Data Format / Common Address		A5	B5	C5	A5	B5	C5	A5	.....	.....	C5	A5	B5	C5
		A4	B4	C4	A4	B4	C4	A4	.....	.....	C4	A4	B4	C4
		A3	B3	C3	A3	B3	C3	A3	.....	.....	C3	A3	B3	C3
		A2	B2	C2	A2	B2	C2	A2	.....	.....	C2	A2	B2	C2
		A1	B1	C1	A1	B1	C1	A1	.....	.....	C1	A1	B1	C1
		A0	B0	C0	A0	B0	C0	A0	.....	.....	C0	A0	B0	C0
Normal	Remapped													
0	127	6	6	6	6	6	6	6	.....	.....	6	6	6	6
1	126	6	6	6	6	6	6	6	.....	.....	6	6	6	6
2	125	6	6	6	6	6	6	6	.....	.....	6	6	6	6
3	124	6	6	6	6	6	6	6	.....	.....	6	6	6	6
4	123	6	6	6	6	6	6	6	.....	.....	6	6	6	6
5	122	6	6	6	6	6	6	6	.....	.....	6	6	6	6
6	121	6	6	no of bits in this cell			6	6	.....	.....	6	6	6	6
7	120								.....	.....	6	6	6	6
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:
:	:	:	:	:	:	:	:	:	.....	.....	:	:	:	:
123	4	6	6	6	6	6	6	6	.....	.....	6	6	6	6
124	3	6	6	6	6	6	6	6	.....	.....	6	6	6	6
125	2	6	6	6	6	6	6	6	.....	.....	6	6	6	6
126	1	6	6	6	6	6	6	6	.....	.....	6	6	6	6
127	0	6	6	6	6	6	6	6	.....	.....	6	6	6	6

Common output
COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
:
:
:
COM124
COM125
COM126
COM127

SEG output	SA0	SB0	SC0	SA1	SB1	SC1	SA2	.....	.....	SC126	SA127	SB127	SC127

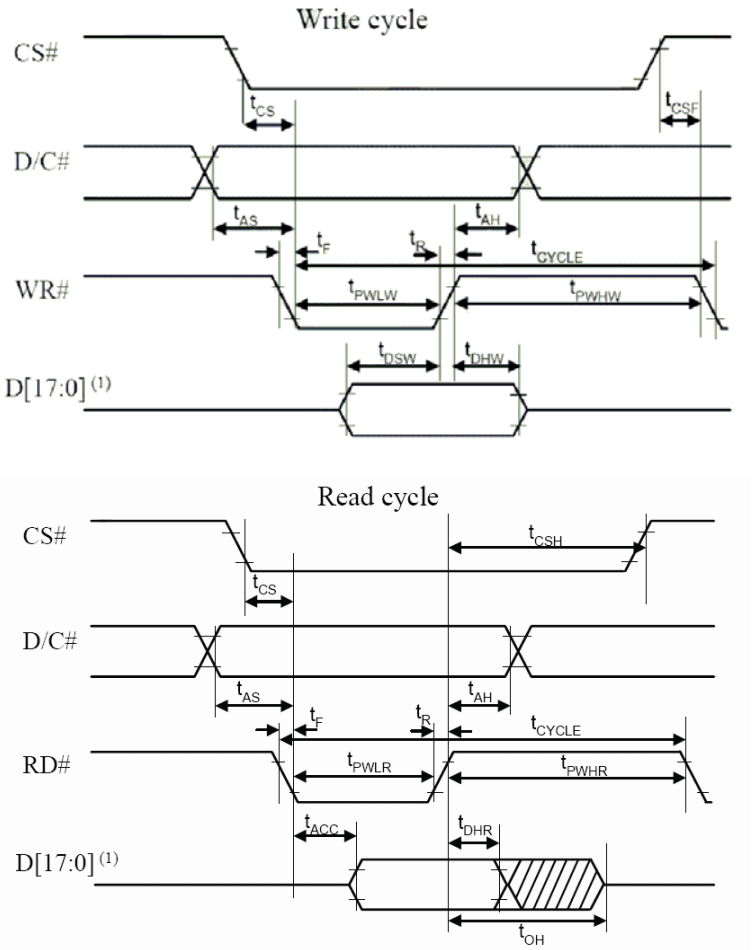
6.5 INTERFACE TIMING CHART

8080-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.65V, V_{CI} = 2.8V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series MCU parallel interface characteristics



Note

(1) when 8 bit used: D[7:0] instead; when 16 bit used: [15:0] instead; when 18 bit used: D[17:0] instead.

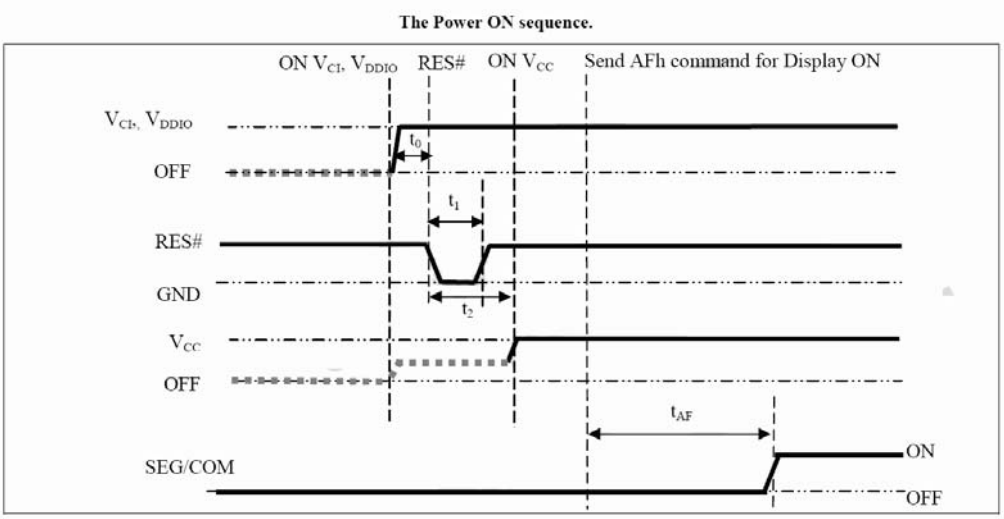
7. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

7.1 POWER ON / OFF SEQUENCE

The following figures illustrate the recommended power ON and power OFF sequence of SSD1351 (assume V_{CI} and V_{DDIO} are at the same voltage level and internal V_{DD} is used).

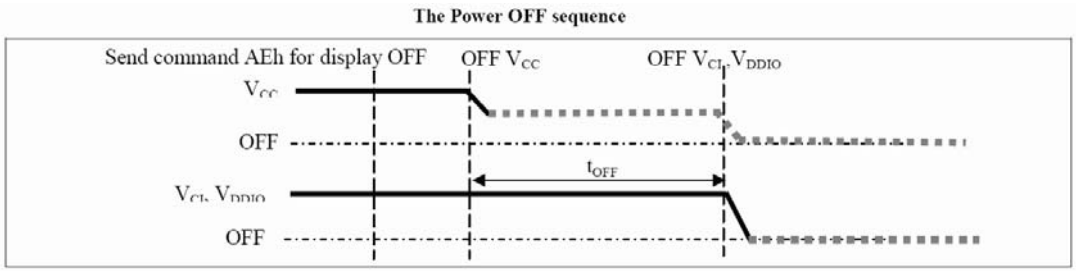
***Power ON sequence*:**

1. Power ON V_{CI}, V_{DDIO}.
2. After V_{CI}, V_{DDIO} become stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 2us (t_1) (4) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 2us (t_2). Then Power ON V_{CC}.(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).



***Power OFF sequence*:**

1. Send command AEh for display OFF.
2. Power OFF V_{CC}.(1), (2)
3. Wait for t_{OFF}. Power OFF V_{CI}, V_{DDIO}.(where Minimum t_{OFF}=80ms (3), Typical t_{OFF}=100ms)



Note:

(1) Since an ESD protection circuit is connected between V_{CI}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{CI} whenever V_{CI}, V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.

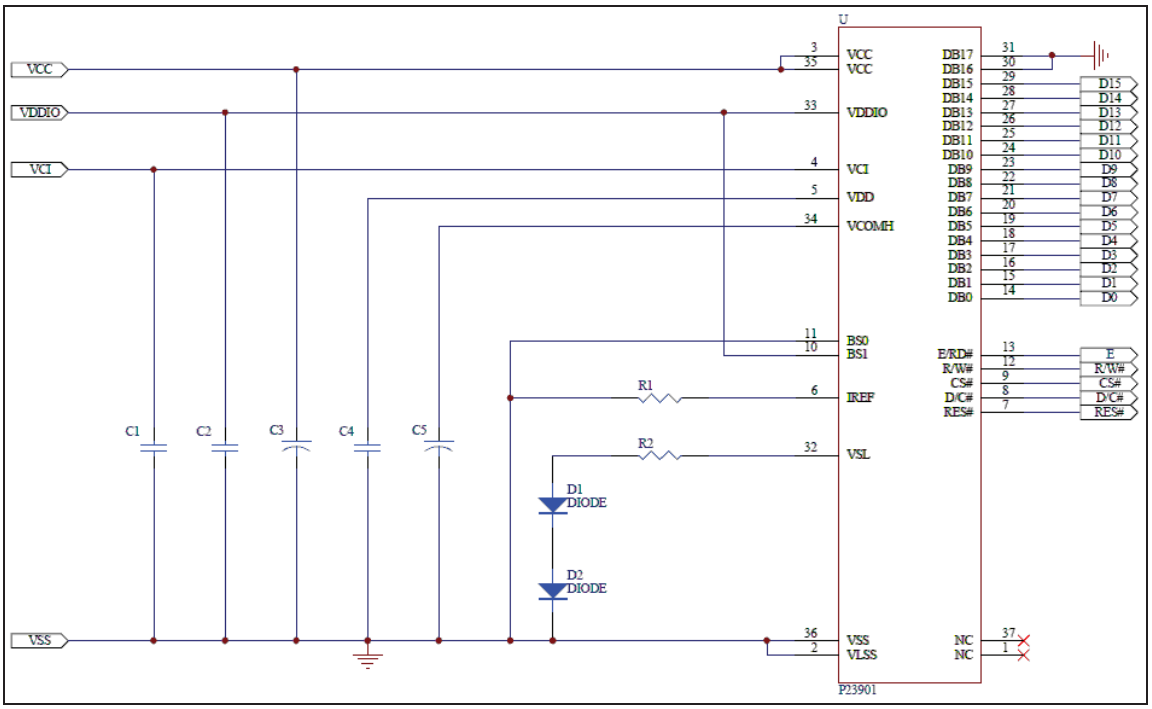
(2) V_{CC} should be kept float (disable) when it is OFF.

(3) V_{CI}, V_{DDIO} should not be Power OFF before V_{CC} Power OFF.

(4) The register values are reset after t_1.

(5) Power pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.

7.2 APPLICATION CIRCUIT



Recommend components:

C1, C2, C4: 1uF/16V(0805)

C3, C5: 4.7uF/35V (Tantalum type) or VISHAY (572D475X0025A2T)

R1: 1M ohm 1%(0603)

R2: 50 ohm 1/4W

D1, D2: RB480K(ROHM)

This circuit is for 8080 16bits interface

7.3COMMANDTABLE

Refer to SSD1351 IC Spec.

7. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	5
2	High temp. (Operation)	70°C, 120hrs	5
3	Low temp. (Operation)	-40°C, 120hrs	5
4	High temp. / High humidity (Operation)	65°C, 90%RH, 96hrs	5
5	Thermal shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 20 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

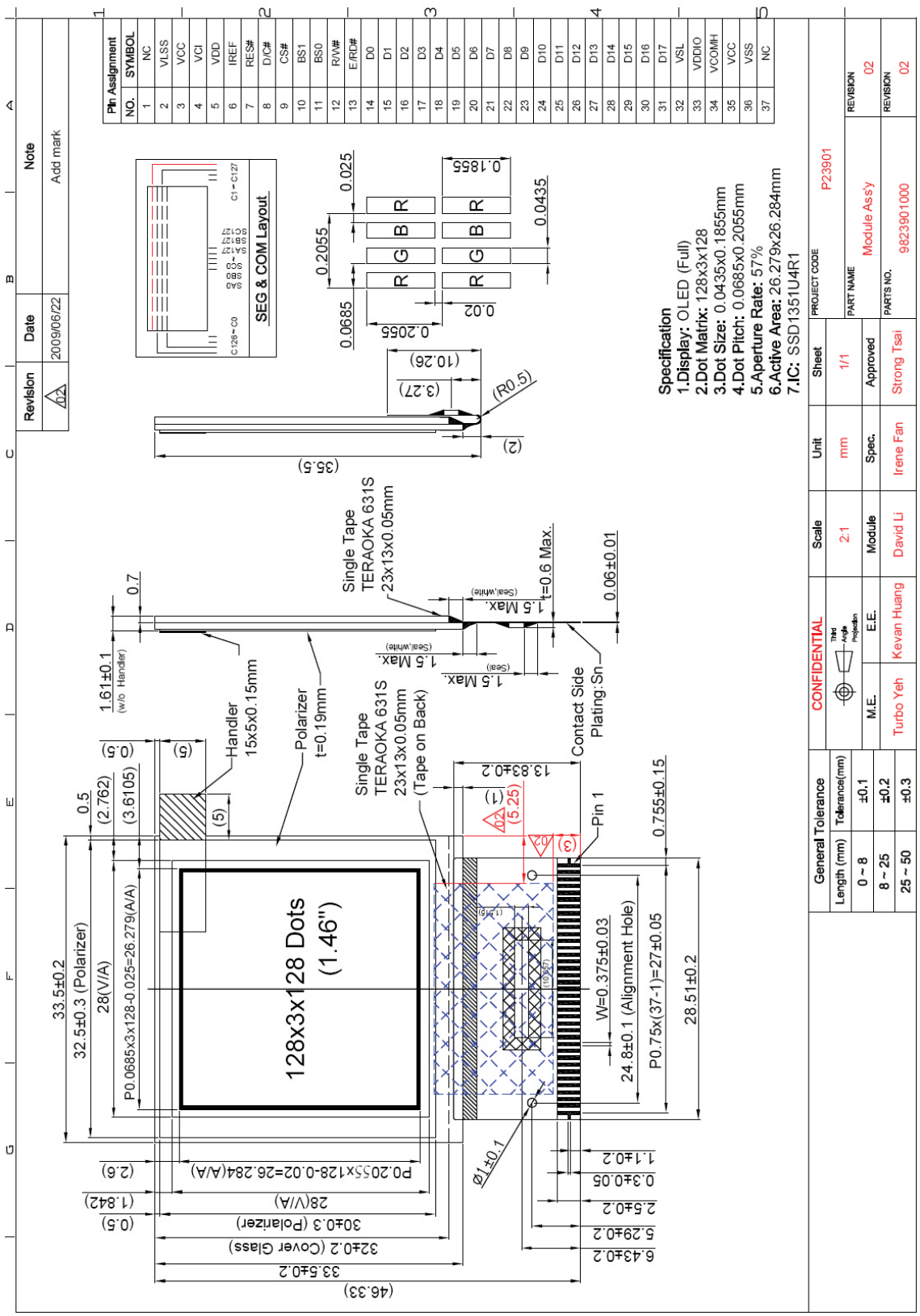
Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

9 . EXTERNAL DIMENSION



11.APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

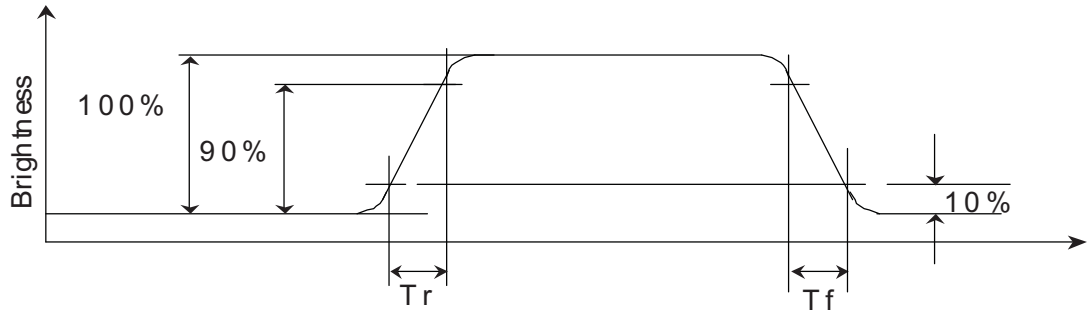


Figure 2: Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

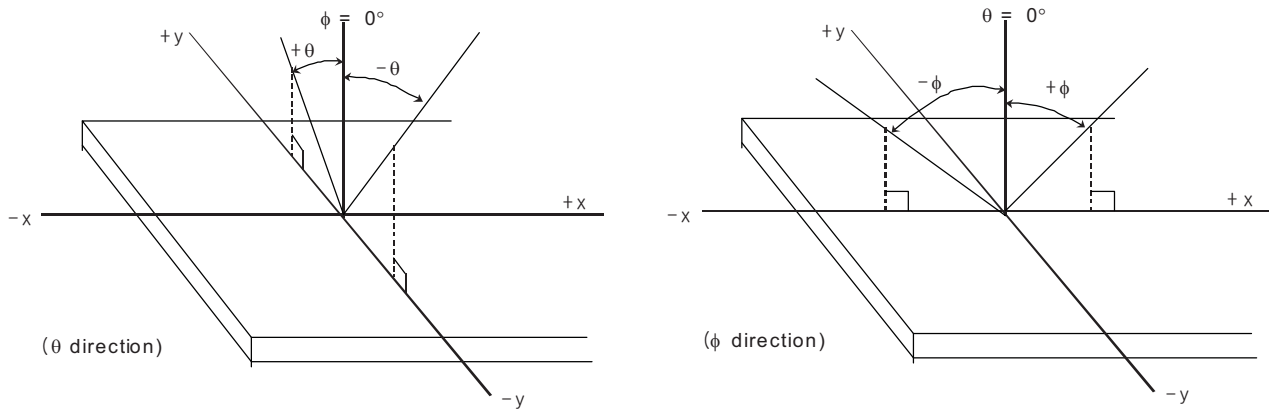
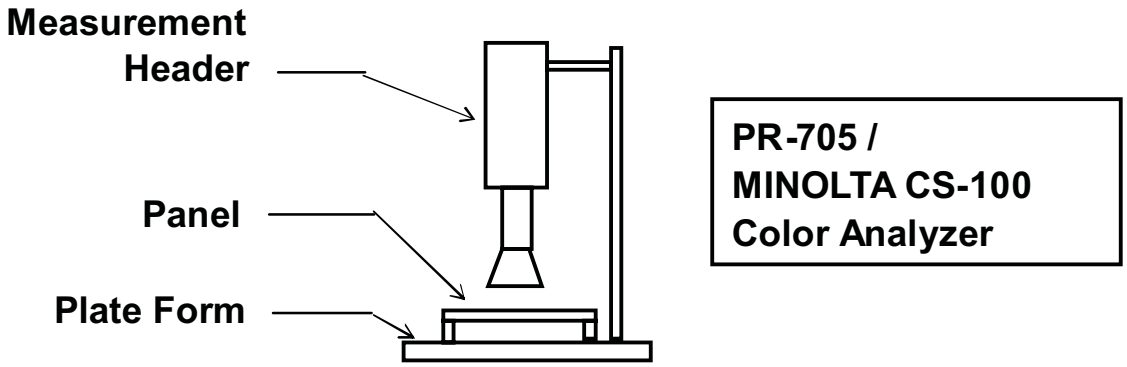


Figure 3: Viewing Angle

APPENDIX 2: MEASUREMENT APPARATUS

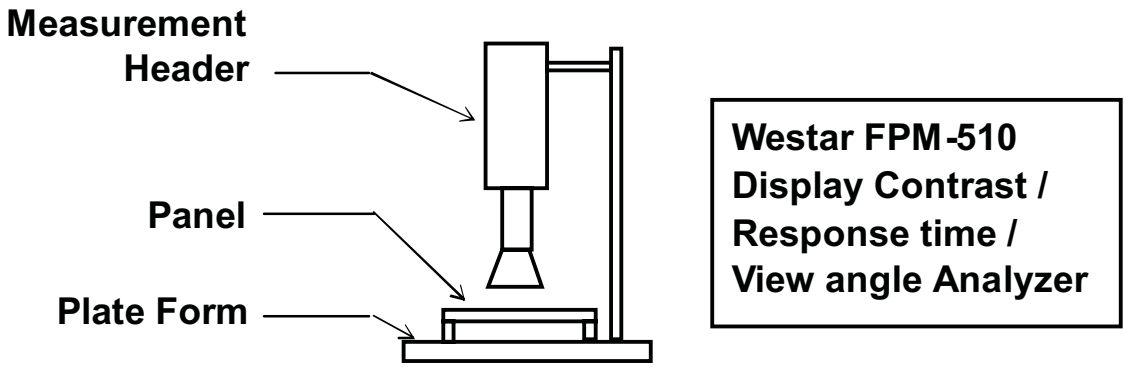
A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100

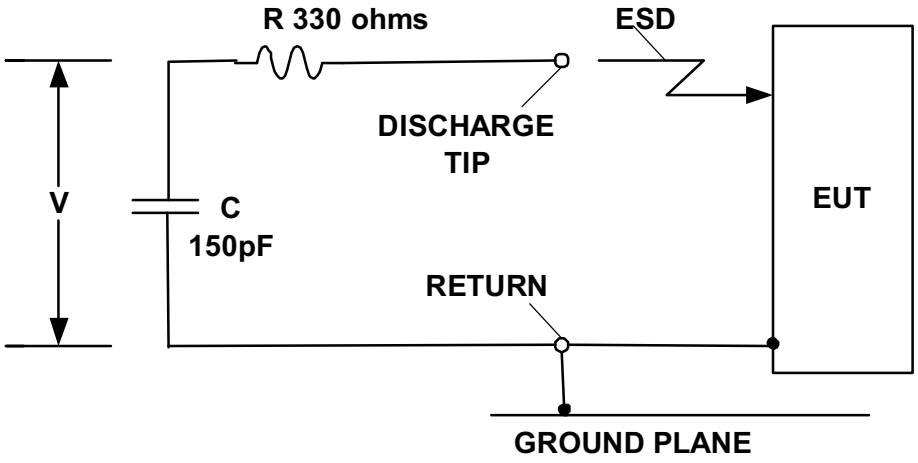


B. CONTRAST / RESPONSE TIME / VIEW ANGLE

WESTAR CORPORATION FPM-510



C. ESD ON AIR DISCHARGE MODE



APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.